

Compal Confidential

DCL55 Schematics Document

Banias ICP uFCBGA/uFCPGA Package with Montara-GM Core Logic

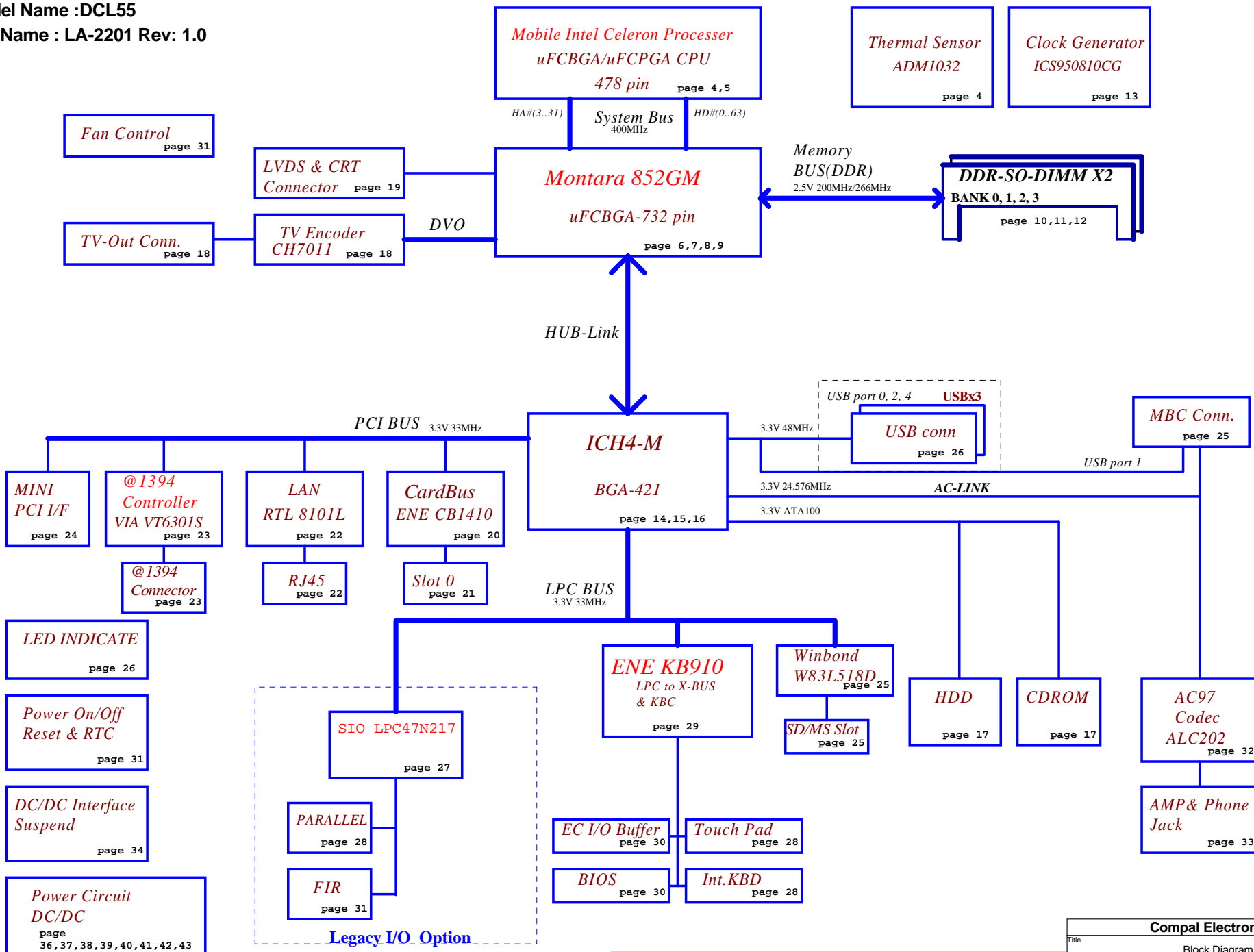
2003-12-29

REV: 1.0

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Title		Cover Sheet	
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	DCL55 LA-2201		1.0
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Model Name :DCL55
File Name : LA-2201 Rev: 1.0



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

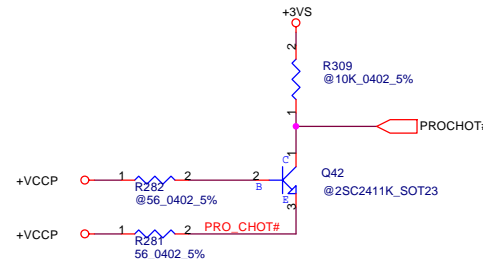
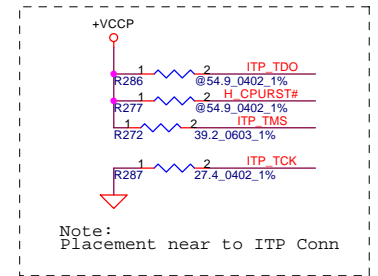
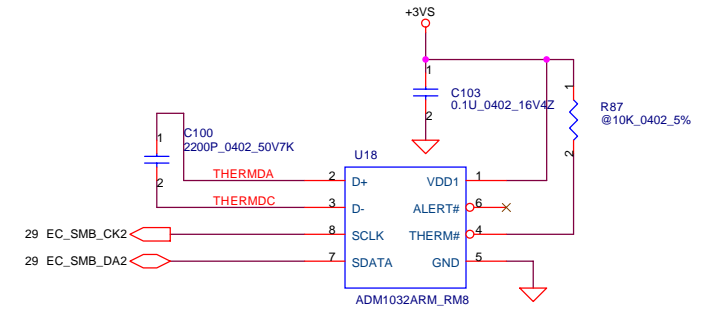
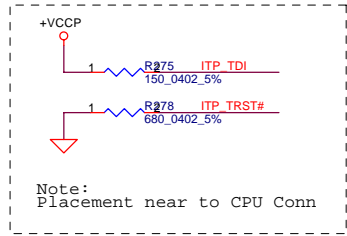
Board ID	PCB Revision
0	0.1
1	0.2
2	1.0
3	
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE

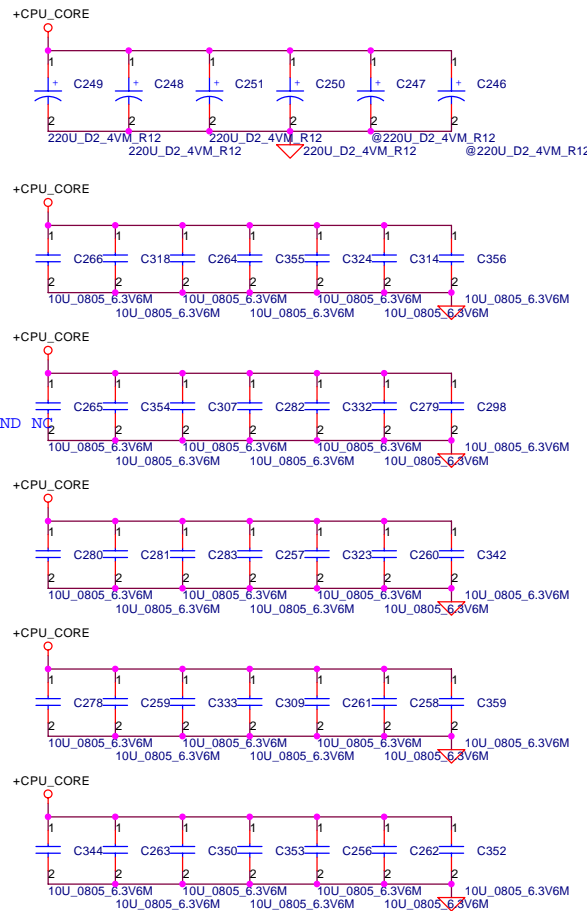
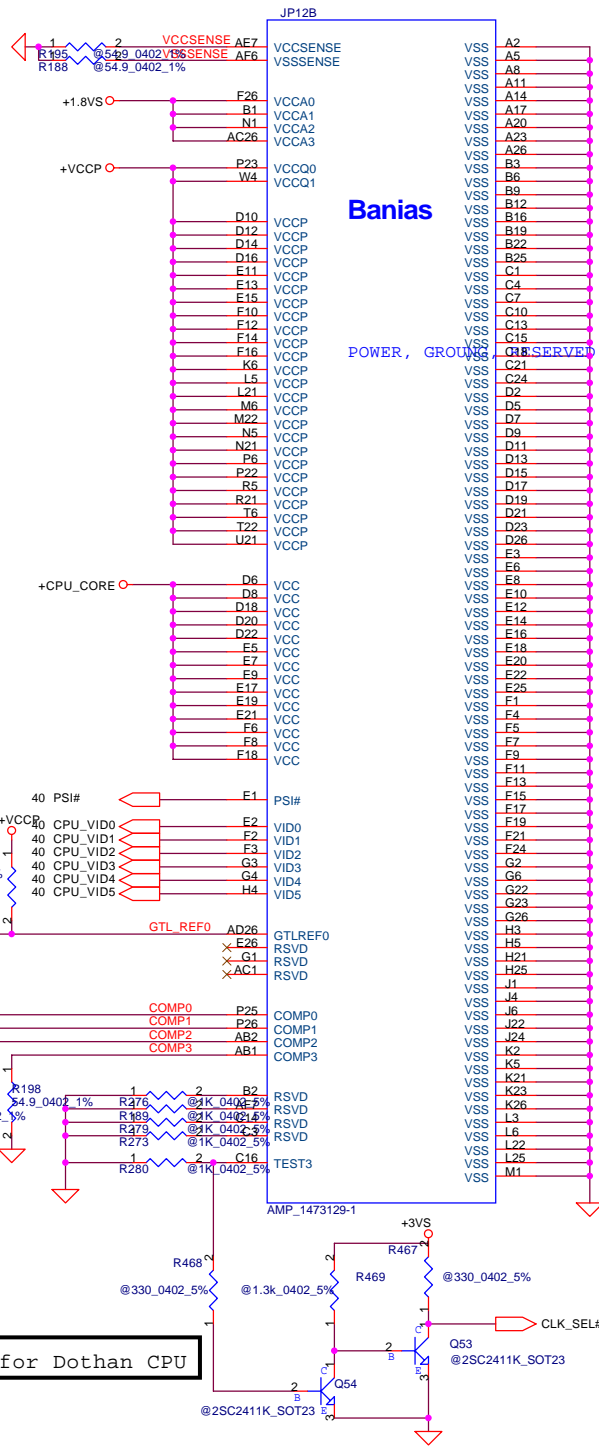
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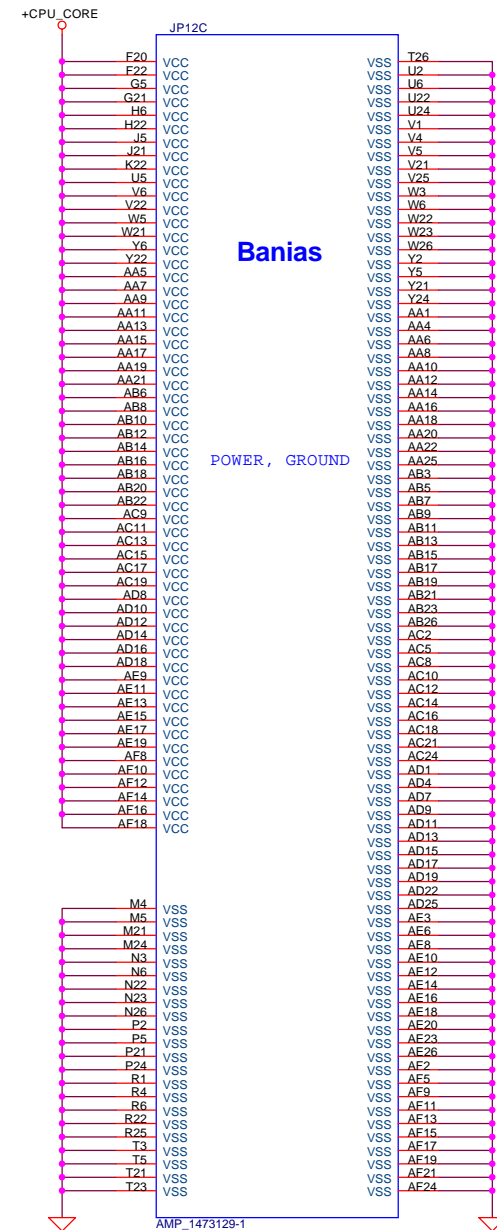
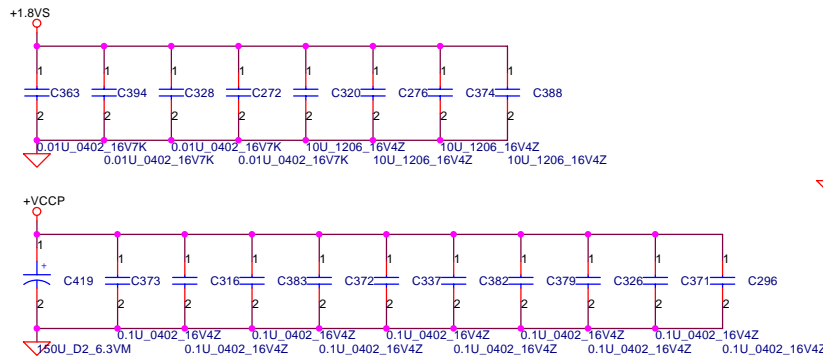


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Banias Processor in mFCPGA479 with ITP			
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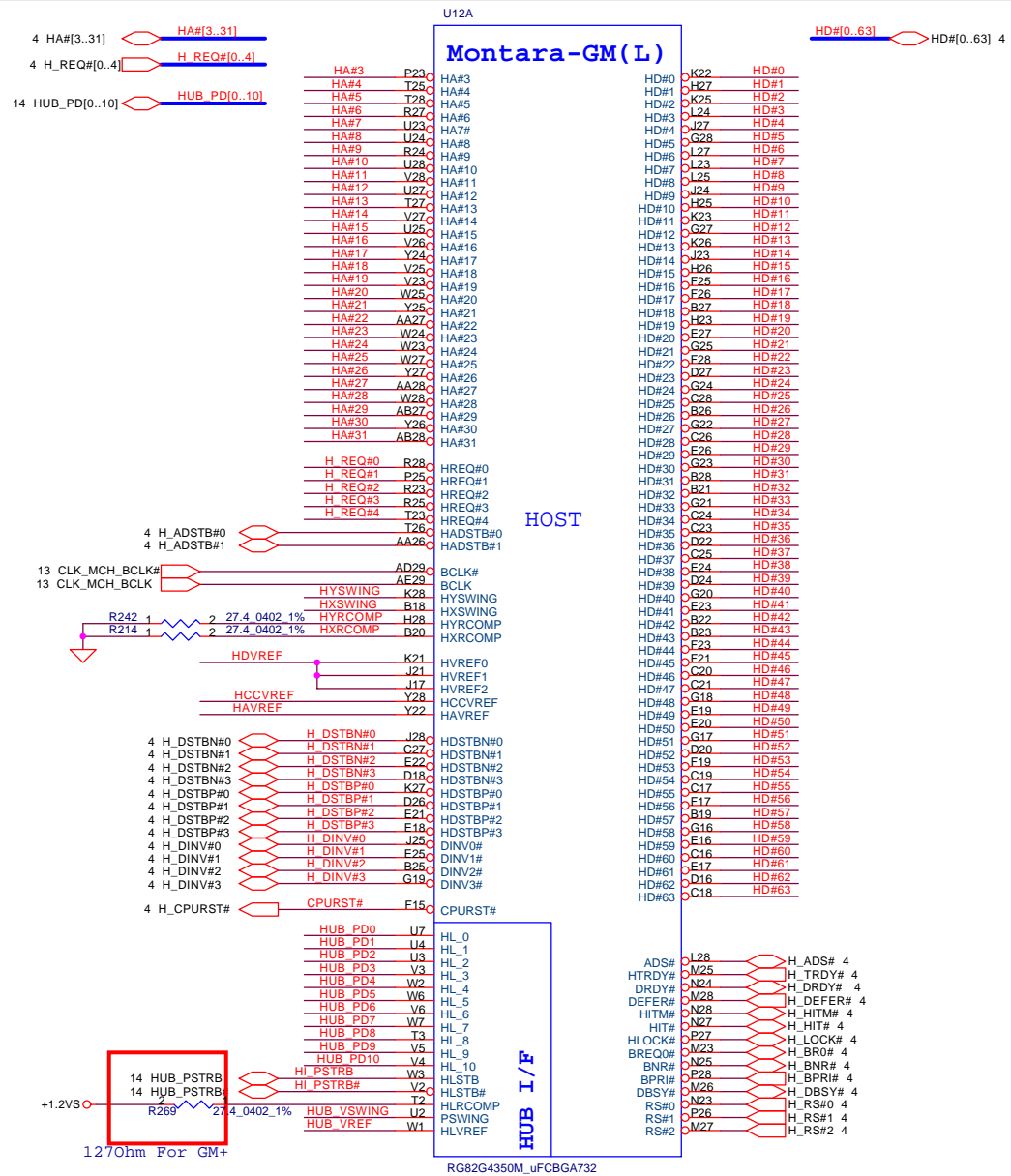


Vcc-core Decoupling	C, uF	ESR, mohm	ESL, nH
SPCAP, Polymer	4X220uF	12m ohm/4	3.5nH/4
MLCC 0805 X5R	35X10uF	5m ohm/35	0.6nH/35

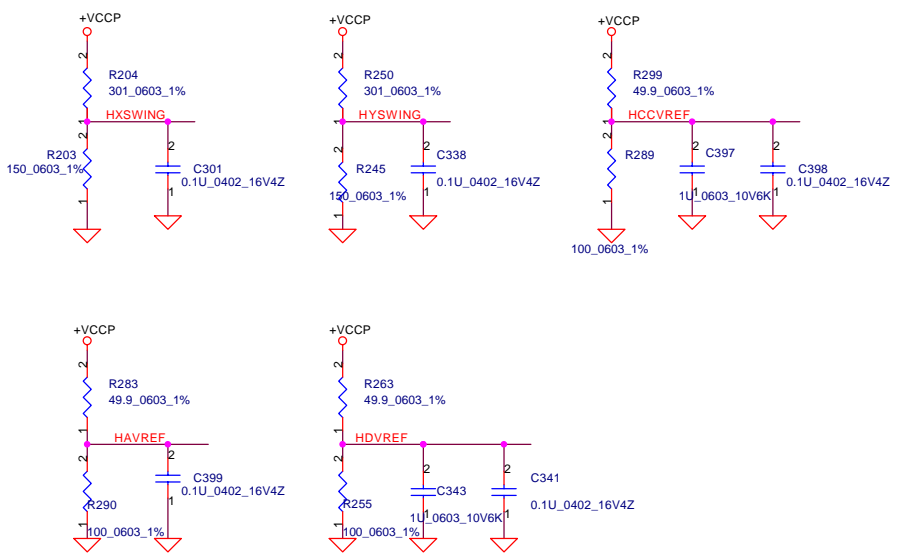


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Title Banias Processor in mFCPGA479		
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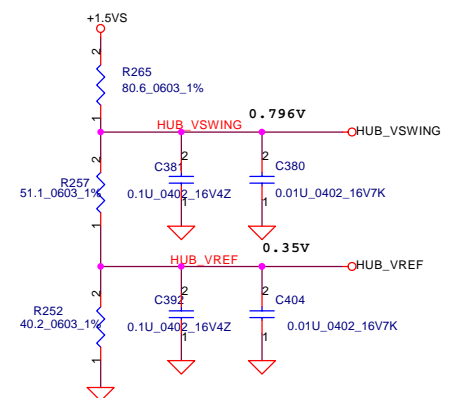
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HOST REF VOLTAGE



HUB I/F REF VOLTAGE



18 DVOC_D[0..11] ← DVOC_D[0..11]

no TV OUT mount R253

DVOCB_CLKINT

R253
100K_0402_5%

18 DVOCB_CLKINT

18 DVOC_CLK

18 DVOC_CLK#

18 DVOC_HSYNC

18 DVOC_VSYNC

18 MI2CCLK

18 MI2CDATA

no TV out mount R466 , Del R251,R235

+1.5VS

R466
1K_0402_5%

DVODETECT

R251
@1K_0603_1%

+1.5VS

10K_0603_1%

15 RTCCCLK

15 AGP_BUSY#

13 CLK_MCH_66M

Montara-GM(L)

DAC

DVO

LVDS

CLKS

MISC

NC

RG82G4350M_uFCBGA732

R3
R5
R6
R4
P6
P5
N5
P2
N2
N3
M1
M5

P3
T6
T5
L2
M2
G2
M3

J3
J2
K6
L5
L3
H5

K7
N6
N7
M6
P7
T7

K5
K1
K3
K2
J6
J5
H2
H1
H4
H6
G3

E5
F5
E3
E2
G5
F4
G6
F6

L7
D5
F1
F7
D1
Y3

AA5
F2
F3
B2
B3
C2
C3
C4
D2
D3
D7
L4

BLUE
BLUE#
GREEN
GREEN#
RED
RED#
HSYNC
VSYNC
REFSET
DDCACLK
DDCADATA

TXOUT0-
TXOUT1-
TXOUT2-
TXOUT0+
TXOUT1+
TXOUT2+
TZOUT0-
TZOUT1-
TZOUT2-
TZOUT0+
TZOUT1+
TZOUT2+

TXCLK-
TXCLK+
TZCLK-
TZCLK+
LCD_CLK
LCD_DATA

INVT_PWM
ENBKL

ENBKL

CLK_MCH_48M
CLK_SSC_66M
CLK_MCH_48M
CLK_SSC_66M

H_DPWR#
H_DPSP#
PCIRST#
VWATE

EXTTS
EXTTS

NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11

1270hm For GM+

R247
127_0603_1%

LCD DC2
R217 2
LCD DD2
R216 2
2.2K_0402_5%
2.2K_0402_5%

+3VS

R222
@510_0402_5%

+3VS

R200
10K_0603_1%

CLK_MCH_48M

R223
@33_0402_5%

C302
@22P_0402_50V8J

CLK_SSC_66M

R211
@33_0402_5%

C284
@22P_0402_50V8J

CLK_MCH_66M

R291
@33_0402_5%

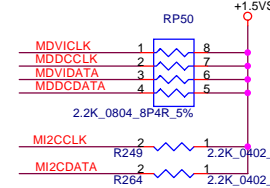
C405
@22P_0402_50V8J

+1.5VS

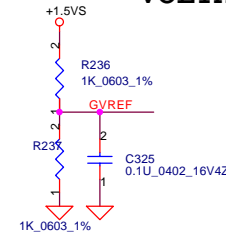
GST0
R227
@1K_0402_5%

GST1
R226
@1K_0402_5%

I2C BUS PULL UP



DVO REF VOLTAGE



Starp pin list

LCLKCTLB: High for P4
N.C. for Banias(default low)
DVODETECT: Low to enable DVO
High to disable DVO

GST0	GST1	PSB/Sys Mem/ GFX Core
0	0	400/266/200 (default)
0	1	400/200/200
1	0	400/200/133

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Title	MONTARA-GM-LVDS(2/4)		
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U12C

Montara-GM(L)

10 DDR_SMA0 DDR_SMA0 AC18 SMA0
10,11 DDR_SMA1 DDR_SMA1 AD14 SMA1
10,11 DDR_SMA2 DDR_SMA2 AD19 SMA2
10 DDR_SMA3 DDR_SMA3 AD17 SMA3
10,11 DDR_SMA4 DDR_SMA4 AC13 SMA4
10,11 DDR_SMA5 DDR_SMA5 AC13 SMA5
DDR_SMA6 AD8 SMA6
DDR_SMA7 AD7 SMA7
DDR_SMA8 AC6 SMA8
DDR_SMA9 AC9 SMA9
DDR_SMA10 AC19 SMA10
DDR_SMA11 AD5 SMA11
DDR_SMA12 AB5 SMA12

DDR_SQ09 AG2 SDQS0
DDR_SQ01 AH5 SDQS1
DDR_SQ02 AH8 SDQS2
DDR_SQ03 AE12 SDQS3
DDR_SQ04 AH17 SDQS4
DDR_SQ05 AE21 SDQS5
DDR_SQ06 AH24 SDQS6
DDR_SQ07 AH27 SDQS7
DDR_SQ08 AD15 SDQS8

10 DDR_SWE# DDR_SWE# AD25 SWE#
10 DDR_SRAS# DDR_SRAS# AC21 SRAS#
10 DDR_SCAS# DDR_SCAS# AC24 SCAS#

10 DDR_CLK0 AB2 SCK0
10 DDR_CLK0# AA2 SCK0#
10 DDR_CLK1 AC26 SCK1
10 DDR_CLK1# AB25 SCK1#
10 DDR_CLK2 AC3 SCK2
11 DDR_CLK3 AC2 SCK2#
11 DDR_CLK3# AD2 SCK3#
11 DDR_CLK4 AB23 SCK4
11 DDR_CLK4# AB24 SCK4#
11 DDR_CLK5 AA3 SCK5
11 DDR_CLK5# AB4 SCK5#

10,11 DDR_CKE0 AC7 SCKE0
10,11 DDR_CKE1 AB7 SCKE1
11 DDR_CKE2 AC9 SCKE2
11 DDR_CKE3 AC10 SCKE3
10,11 DDR_SCS#0 AD23 SCS#0
10,11 DDR_SCS#1 AD26 SCS#1
11 DDR_SCS#2 AC22 SCS#2
11 DDR_SCS#3 AC25 SCS#3

10 DDR_SBS0 DDR_SBS0 AD22 SBA0
10 DDR_SBS1 DDR_SBS1 AD20 SBA1

DDR_SDM0 AE5 SDM0
DDR_SDM1 AE6 SDM1
DDR_SDM2 AE9 SDM2
DDR_SDM3 AH12 SDM3
DDR_SDM4 AD19 SDM4
DDR_SDM5 AD21 SDM5
DDR_SDM6 AD24 SDM6
DDR_SDM7 AH28 SDM7
DDR_SDM8 AH15 SDM8

11 DDR_SMA_B1 DDR_SMA_B1 AD16 SMA_B1
11 DDR_SMA_B2 DDR_SMA_B2 AC12 SMA_B2
11 DDR_SMA_B4 DDR_SMA_B4 AF11 SMA_B4
11 DDR_SMA_B5 DDR_SMA_B5 AD10 SMA_B5

AC15# RCVENOUT#
AC16# RCVENIN#
MRCOMP AB1 SMRCOMP
MVSWINGL AJ22 SMVSWINGL
MVSWINGH AJ19 SMVSWINGH

RG82G4350M_uFCBGA732

MEMORY

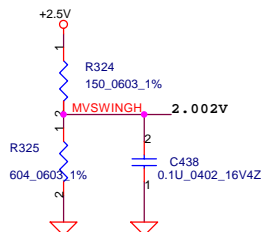
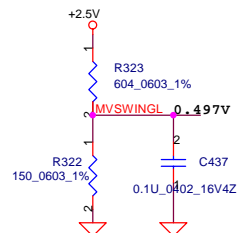
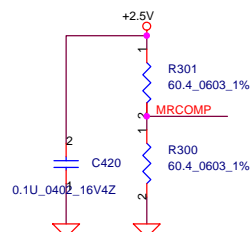
SDQ0 AF2 DDR_SQ00
SDQ1 AE3 DDR_SQ01
SDQ2 AF4 DDR_SQ02
SDQ3 AH2 DDR_SQ03
SDQ4 AD3 DDR_SQ04
SDQ5 AE2 DDR_SQ05
SDQ6 AG4 DDR_SQ06
SDQ7 AH3 DDR_SQ07
SDQ8 AD6 DDR_SQ08
SDQ9 AG5 DDR_SQ09
SDQ10 AE7 DDR_SQ10
SDQ11 AG8 DDR_SQ11
SDQ12 AH4 DDR_SQ12
SDQ13 AF5 DDR_SQ13
SDQ14 AH6 DDR_SQ14
SDQ15 AE8 DDR_SQ15
SDQ16 AG9 DDR_SQ16
SDQ17 AH9 DDR_SQ17
SDQ18 AG10 DDR_SQ18
SDQ19 AH7 DDR_SQ19
SDQ20 AD9 DDR_SQ20
SDQ21 AF10 DDR_SQ21
SDQ22 AE11 DDR_SQ22
SDQ23 AH10 DDR_SQ23
SDQ24 AG11 DDR_SQ24
SDQ25 AH11 DDR_SQ25
SDQ26 AG13 DDR_SQ26
SDQ27 AF14 DDR_SQ27
SDQ28 AG11 DDR_SQ28
SDQ29 AD12 DDR_SQ29
SDQ30 AE13 DDR_SQ30
SDQ31 AH13 DDR_SQ31
SDQ32 AH16 DDR_SQ32
SDQ33 AG17 DDR_SQ33
SDQ34 AF19 DDR_SQ34
SDQ35 AD18 DDR_SQ35
SDQ36 AE18 DDR_SQ36
SDQ37 AH18 DDR_SQ37
SDQ38 AG19 DDR_SQ38
SDQ39 AH20 DDR_SQ39
SDQ40 AG20 DDR_SQ40
SDQ41 AF22 DDR_SQ41
SDQ42 AE22 DDR_SQ42
SDQ43 AH19 DDR_SQ43
SDQ44 AG21 DDR_SQ44
SDQ45 AH21 DDR_SQ45
SDQ46 AG22 DDR_SQ46
SDQ47 AE23 DDR_SQ47
SDQ48 AH23 DDR_SQ48
SDQ49 AE24 DDR_SQ49
SDQ50 AH25 DDR_SQ50
SDQ51 AG25 DDR_SQ51
SDQ52 AE23 DDR_SQ52
SDQ53 AG23 DDR_SQ53
SDQ54 AF23 DDR_SQ54
SDQ55 AG25 DDR_SQ55
SDQ56 AE26 DDR_SQ56
SDQ57 AG28 DDR_SQ57
SDQ58 AF28 DDR_SQ58
SDQ59 AG26 DDR_SQ59
SDQ60 AE26 DDR_SQ60
SDQ61 AE27 DDR_SQ61
SDQ62 AD27 DDR_SQ62
SDQ63 AD27 DDR_SQ63

SDQ64 AG14 DDR_CB0
SDQ65 AE14 DDR_CB1
SDQ66 AG16 DDR_CB2
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SDQ69 AF16 DDR_CB5
SDQ70 AF17 DDR_CB6
SDQ71 AF17 DDR_CB7

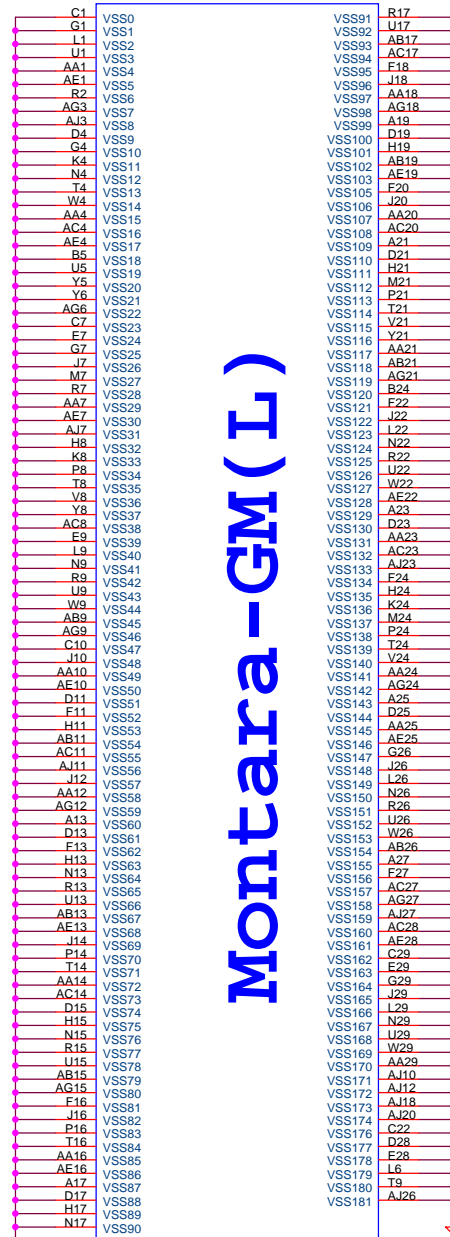
SMVREF0 AJ24

C436 0.1U_0402_16V4Z

DDR REF & SWING VOLTAGE



U12D



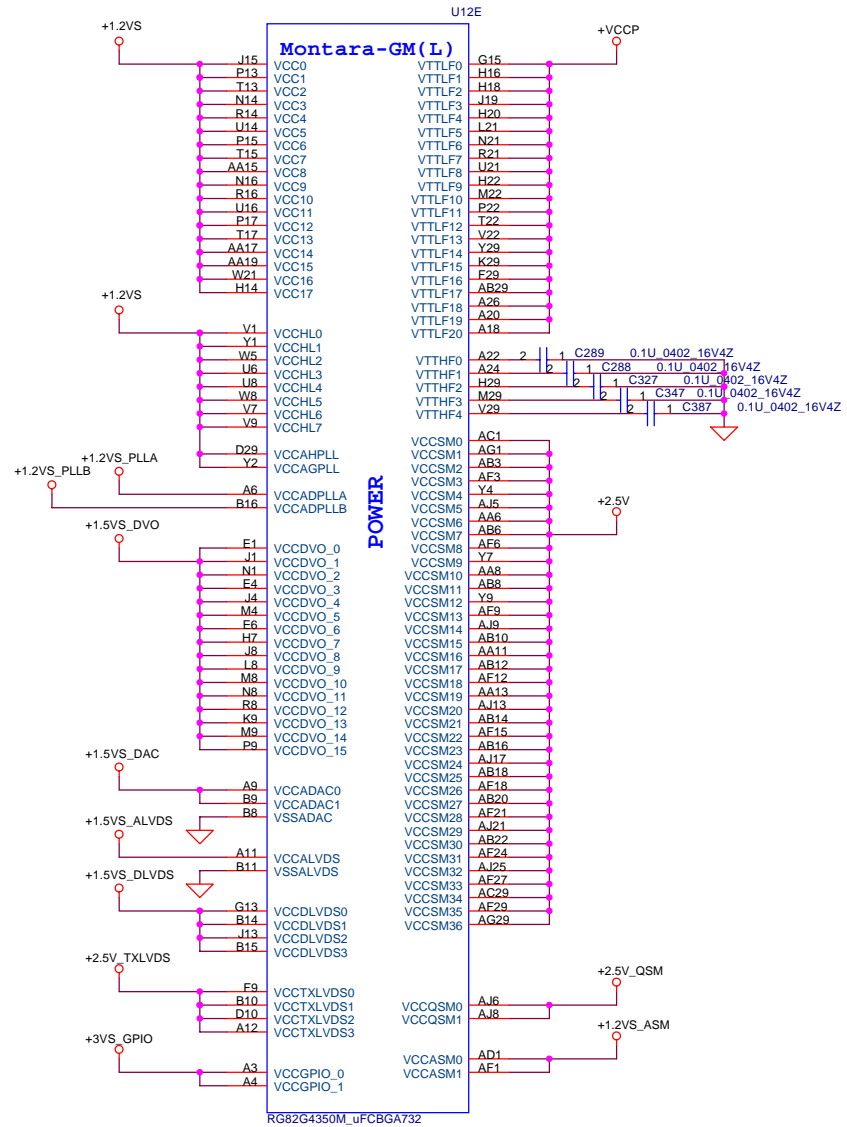
RG82G4350M_uFCBGA732

Montara-GM(L)

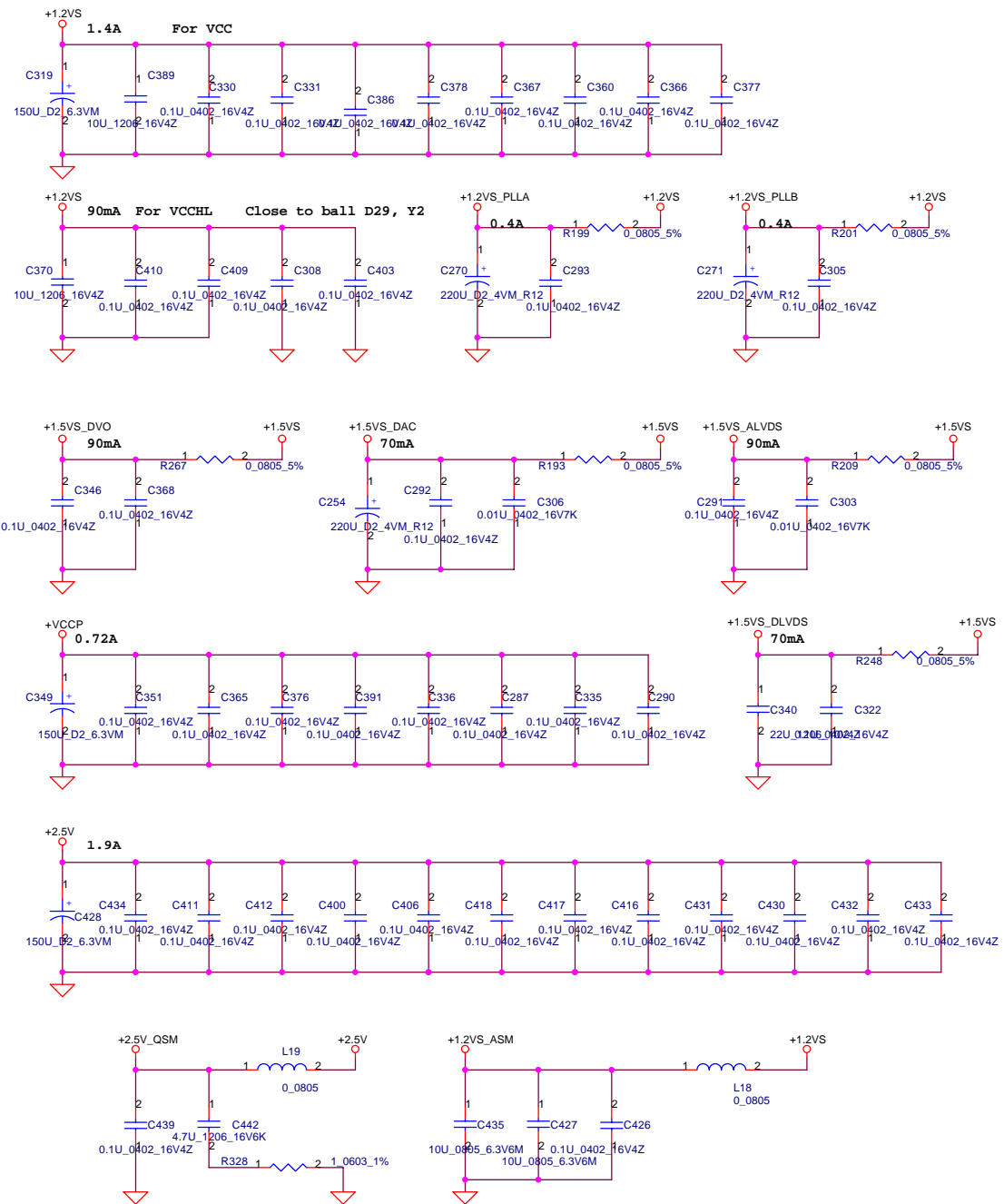
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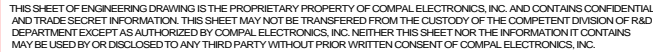
POWER



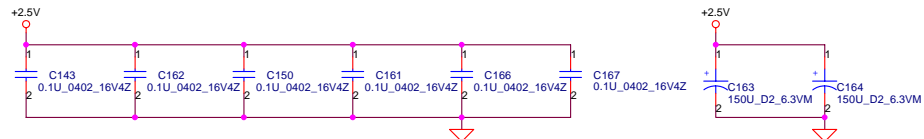
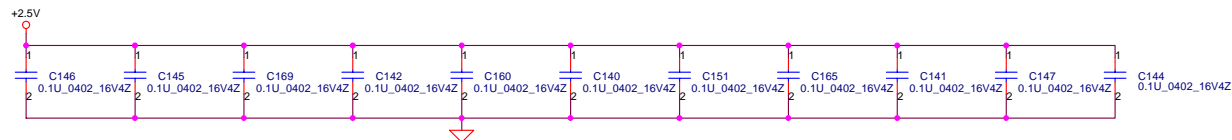
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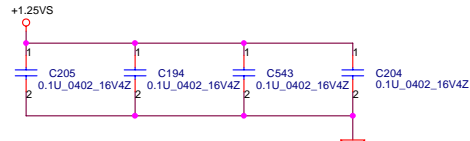
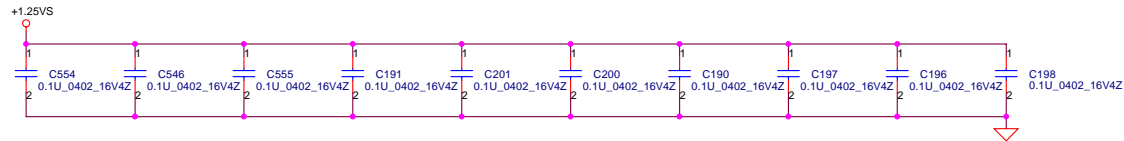
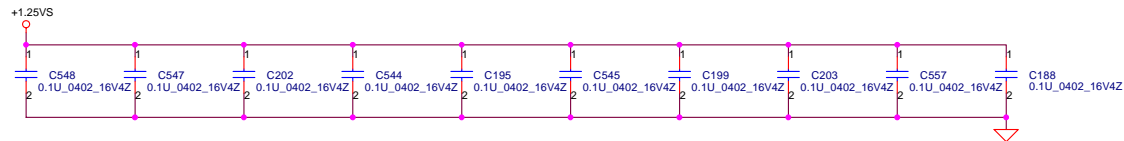
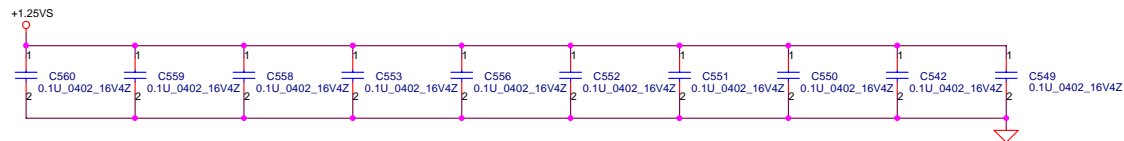
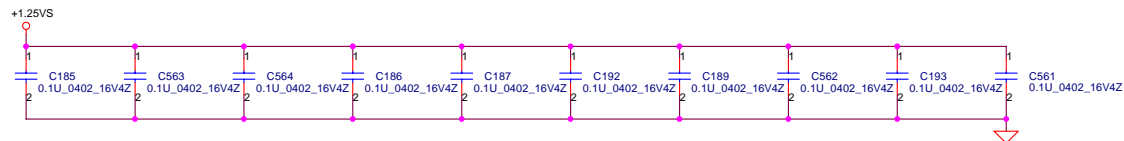
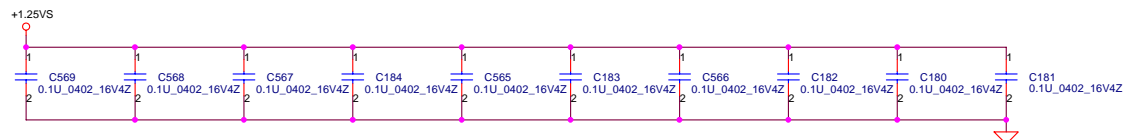
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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Title			
DDR SODIMM Decoupling			
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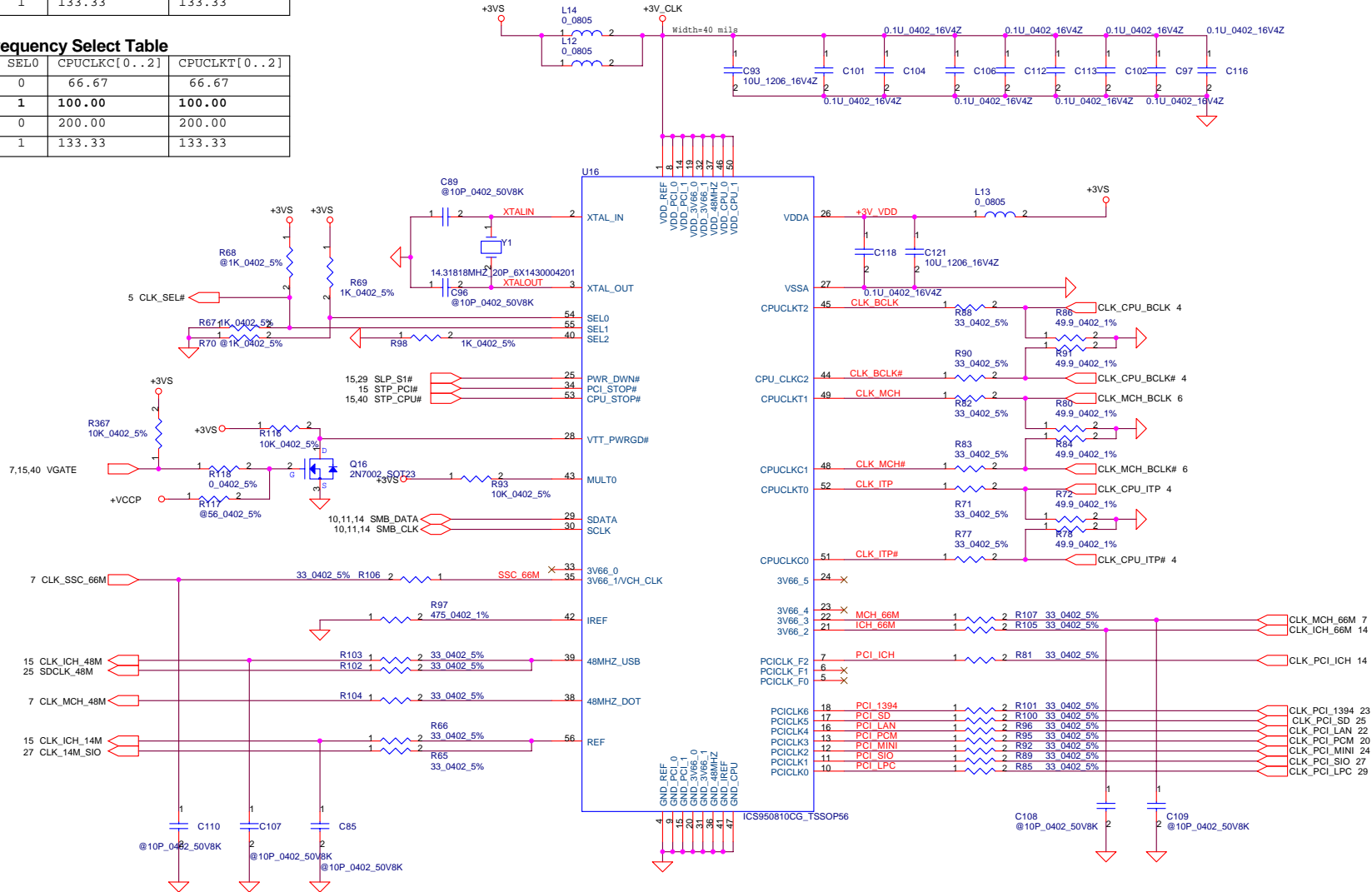
ICS950810 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

CY28346-2 Frequency Select Table

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

Clock Generator



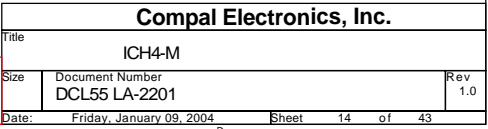
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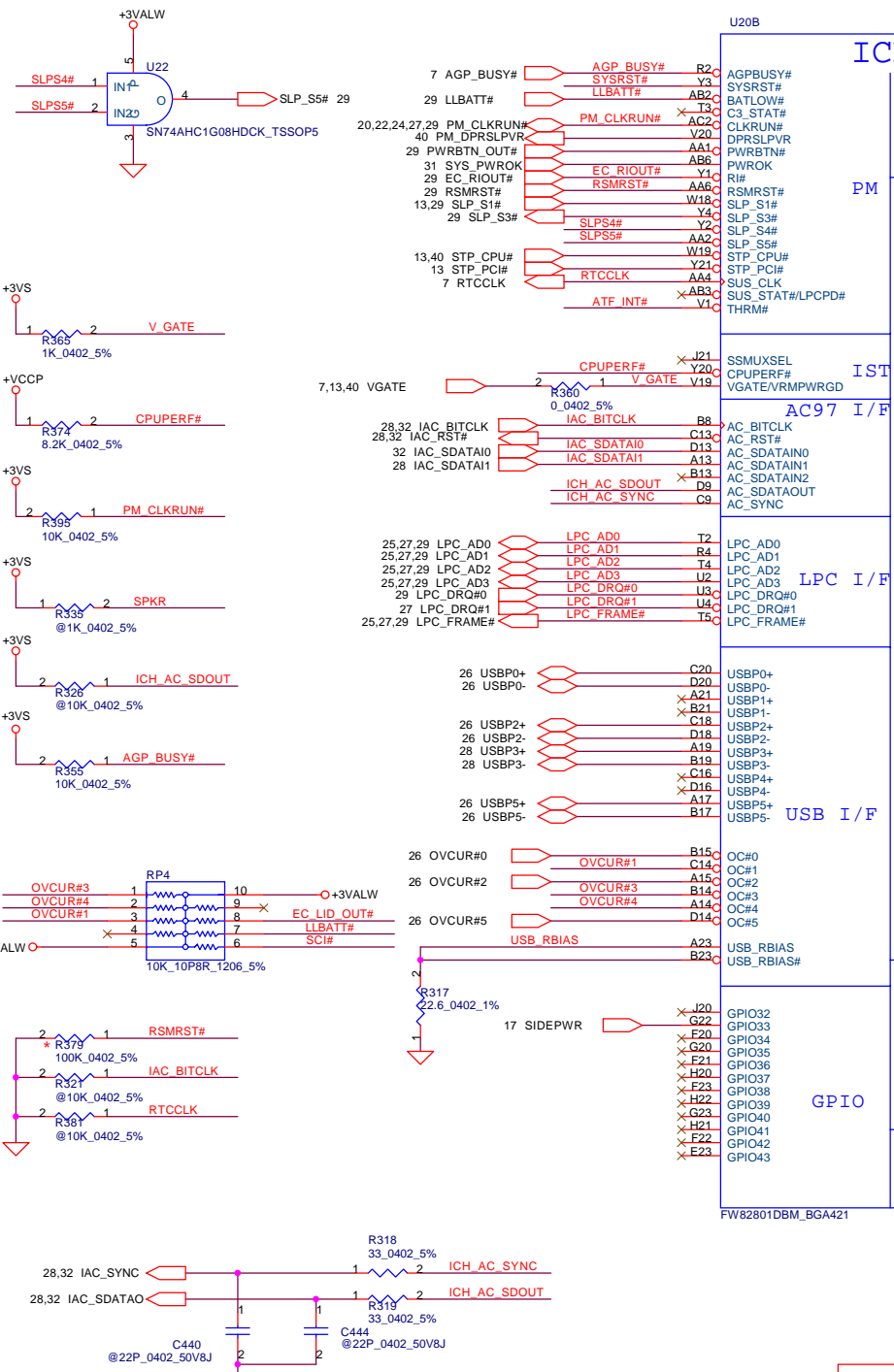
Compal Electronics, Inc.

Clock Generator

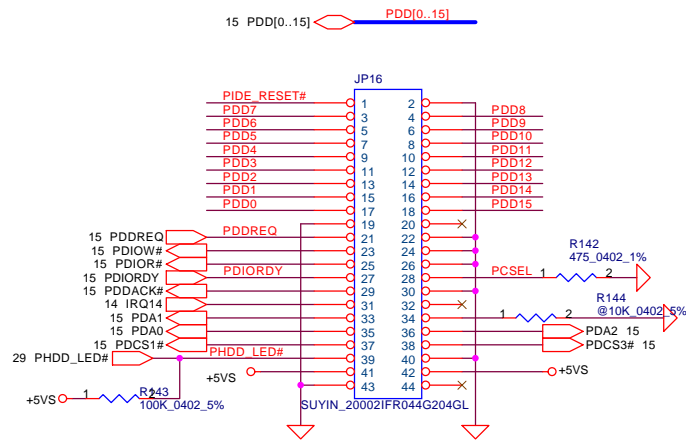
Size	Document Number	Rev
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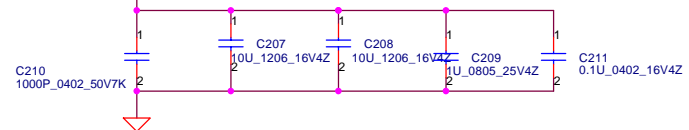




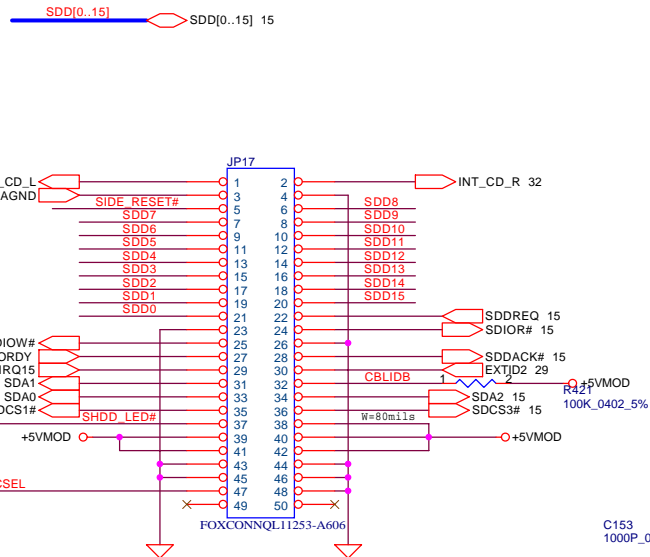
HDD Connector



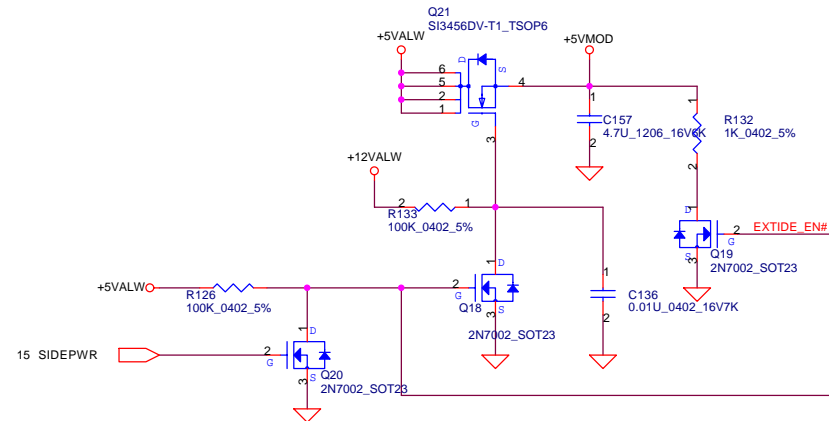
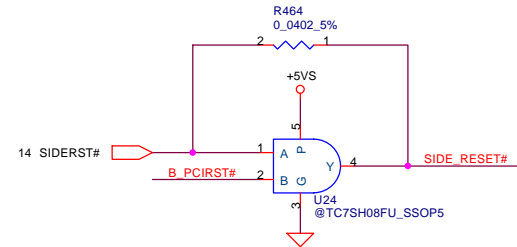
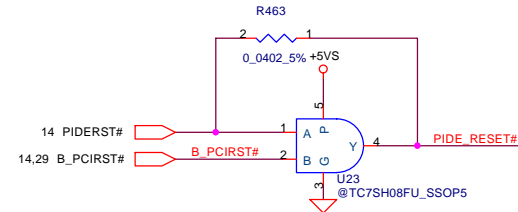
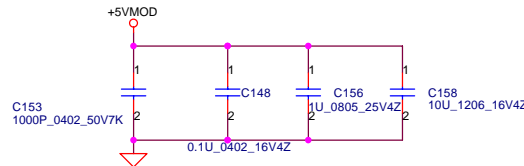
Placea caps. near HDD
CONN.



CD-ROM Connector



Placea caps. near CDROM
CONN.



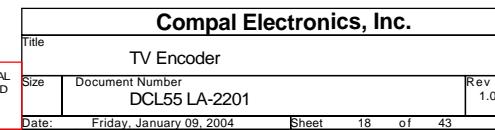
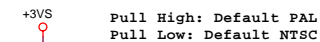
SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

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Compal Electronics, Inc.

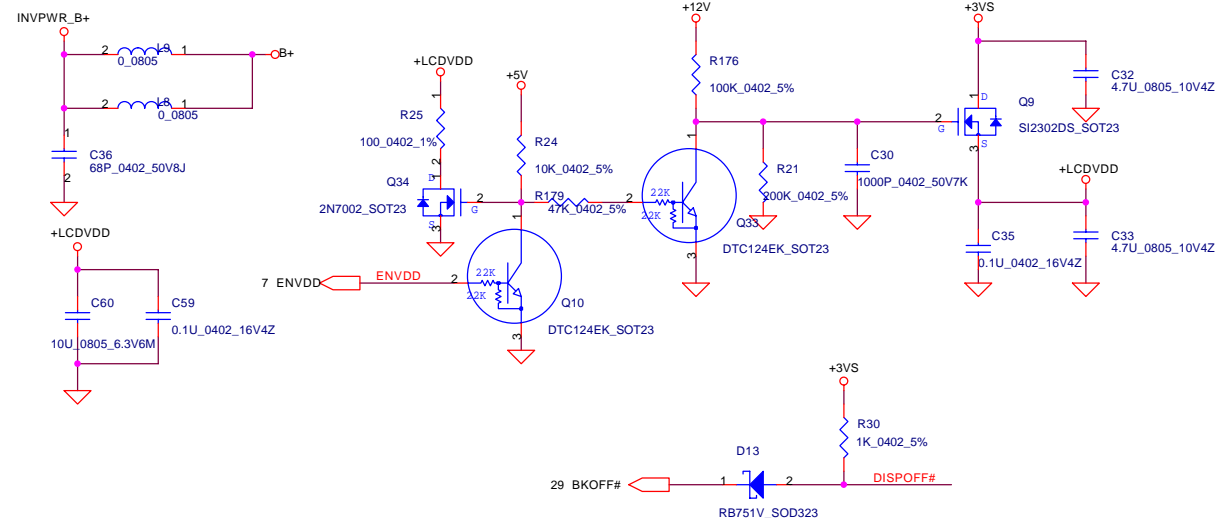
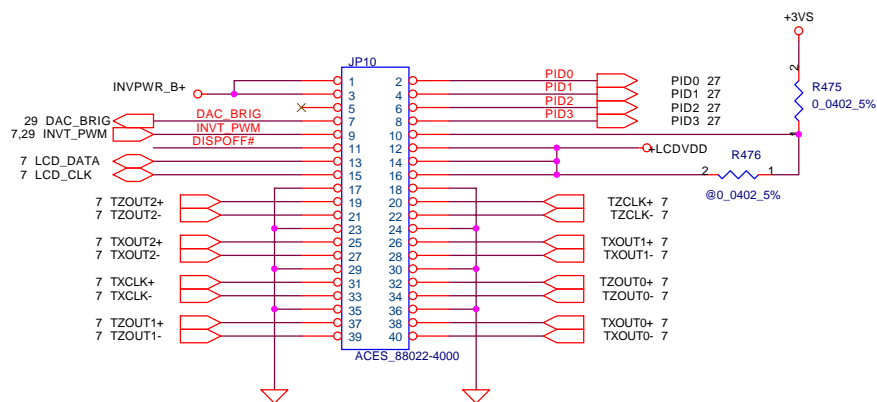
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IDE/CD-ROM Module		
Size	Document Number	Rev
	DCL55 LA-2201	1.0
Date:	Friday, January 09, 2004	Sheet 17 of 43

TV Encoder

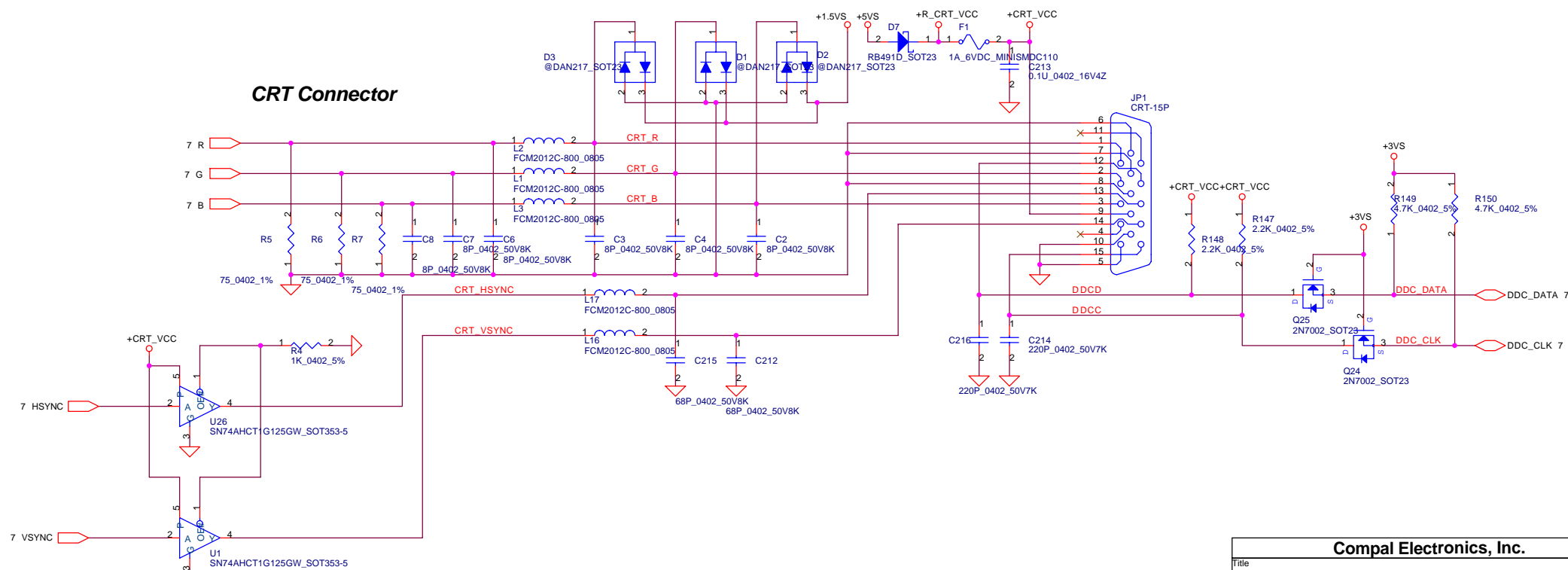


WWW.AliSaler.Com

LVDS Connector

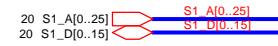
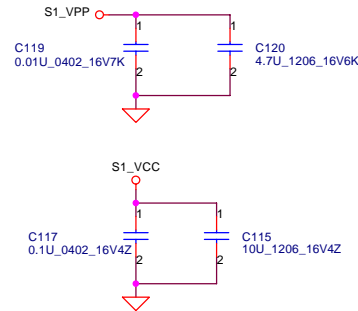
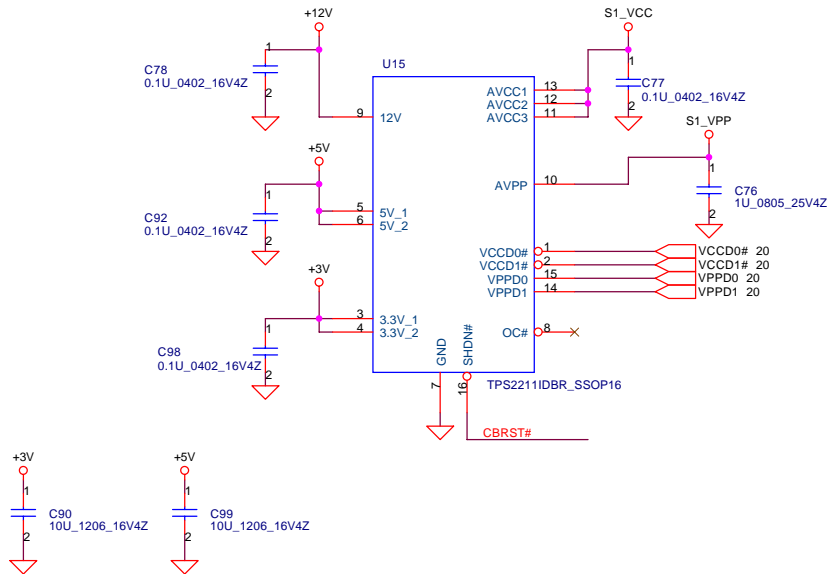


CRT Connector

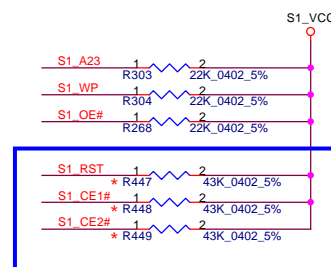
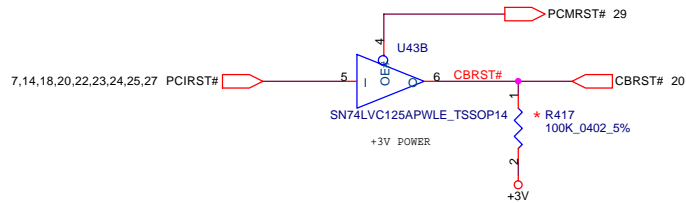
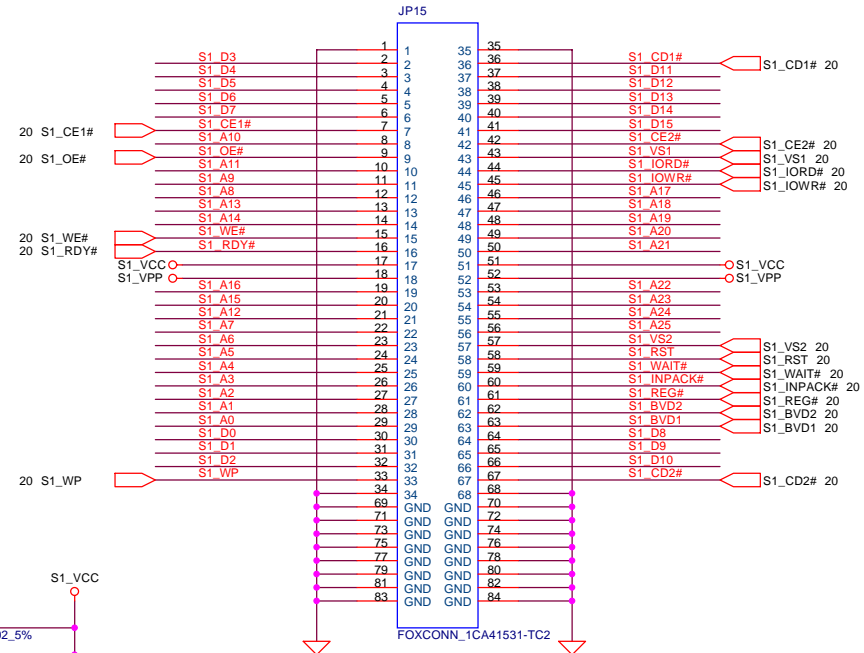


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PCMCIA Power Controller



CardBus Socket



Reserve for CB1410 B0 Version

Compal Electronics, Inc.

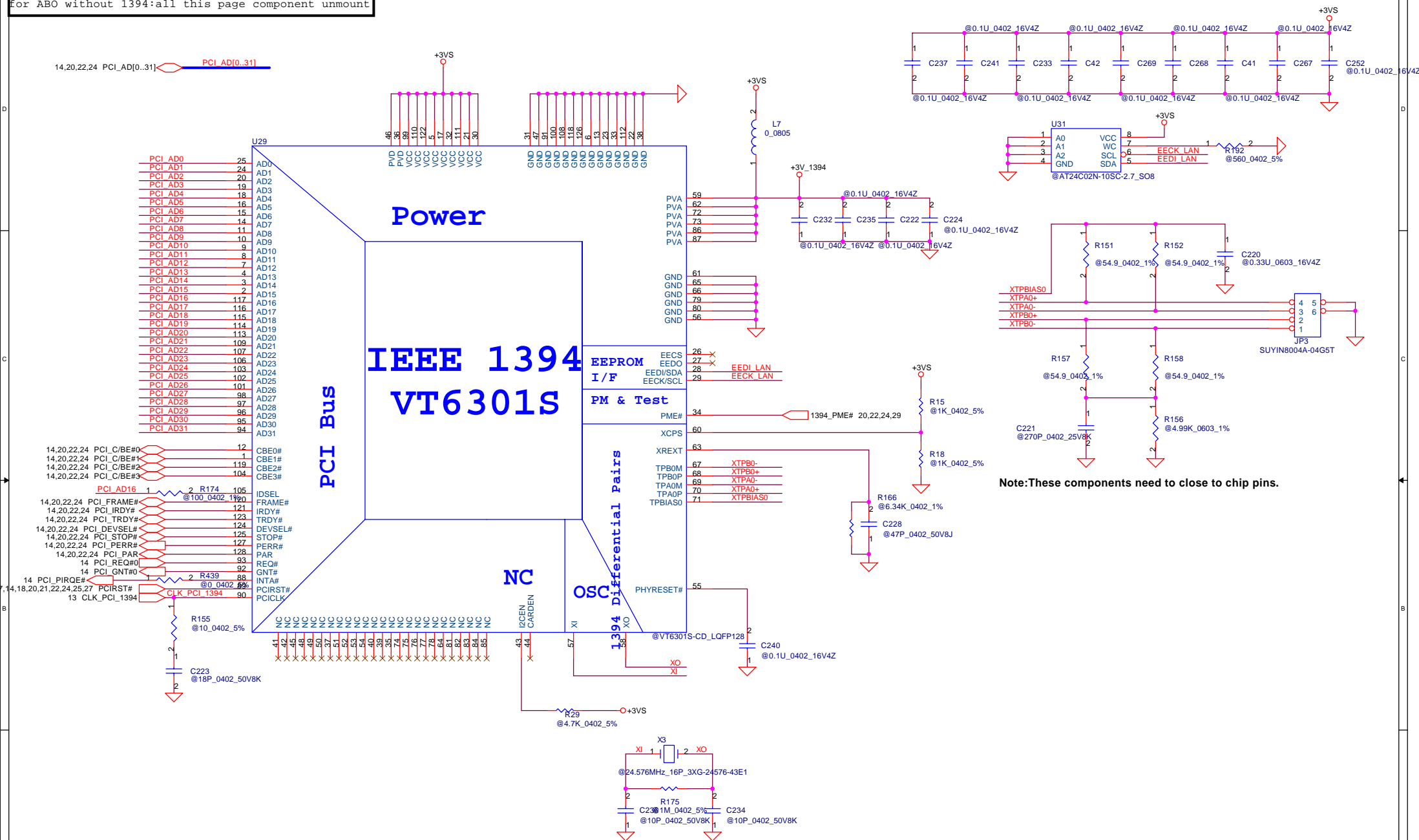
CardBus Socket

DCL55 LA-2201

Title		
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for ABO without 1394:all this page component unmount
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Compal Electronics, Inc.

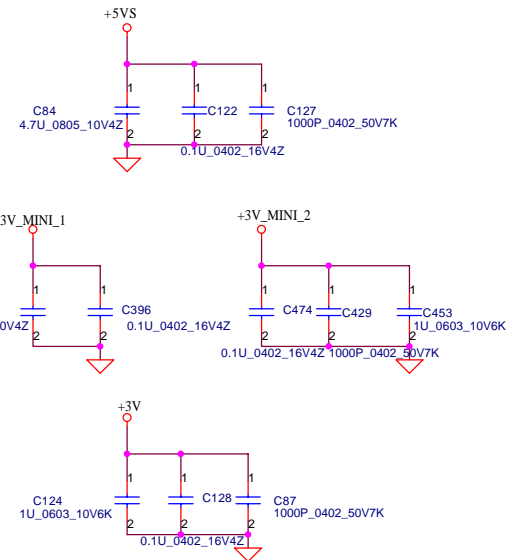
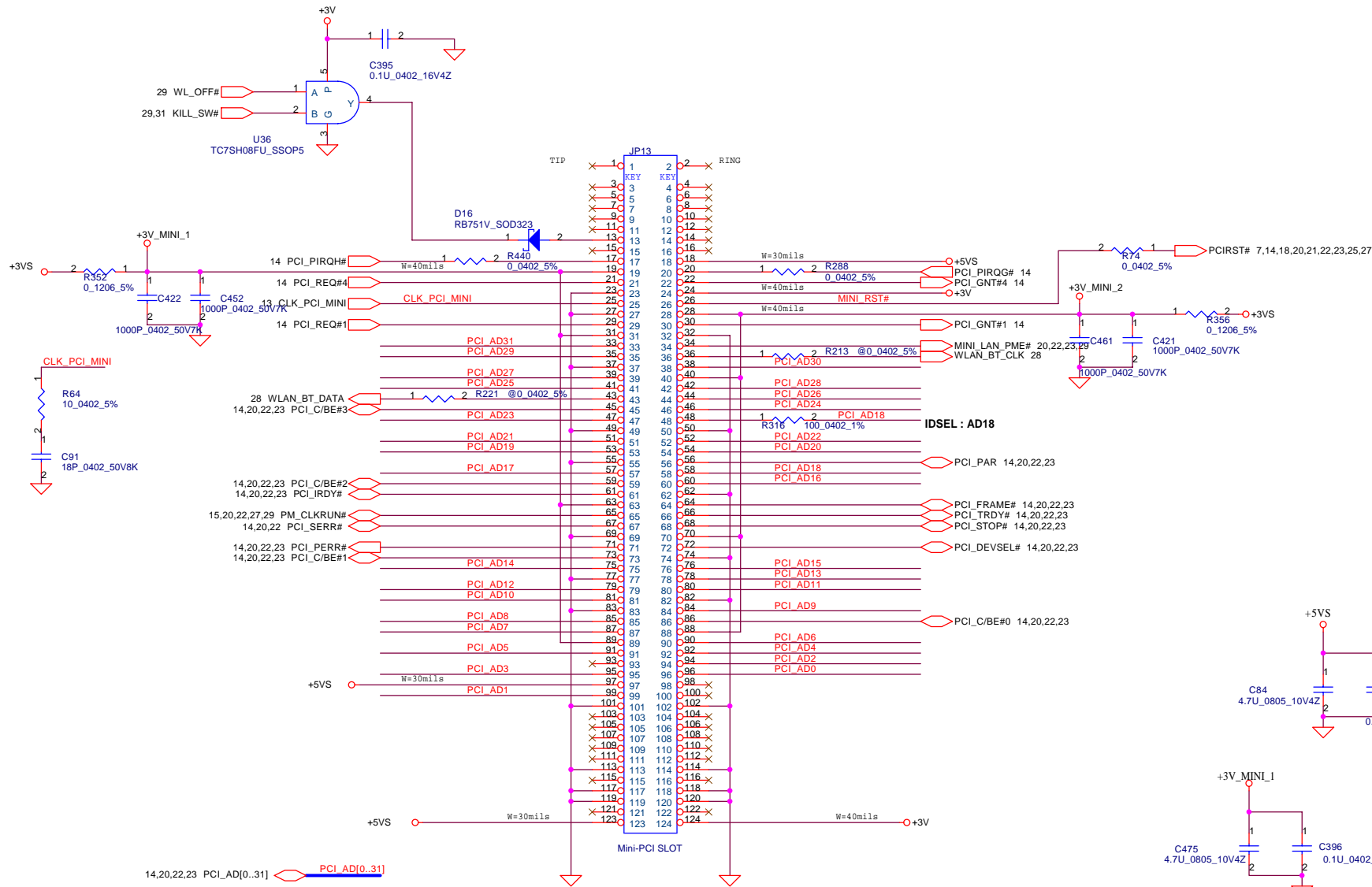
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Size	Document Number
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Rev	1.0
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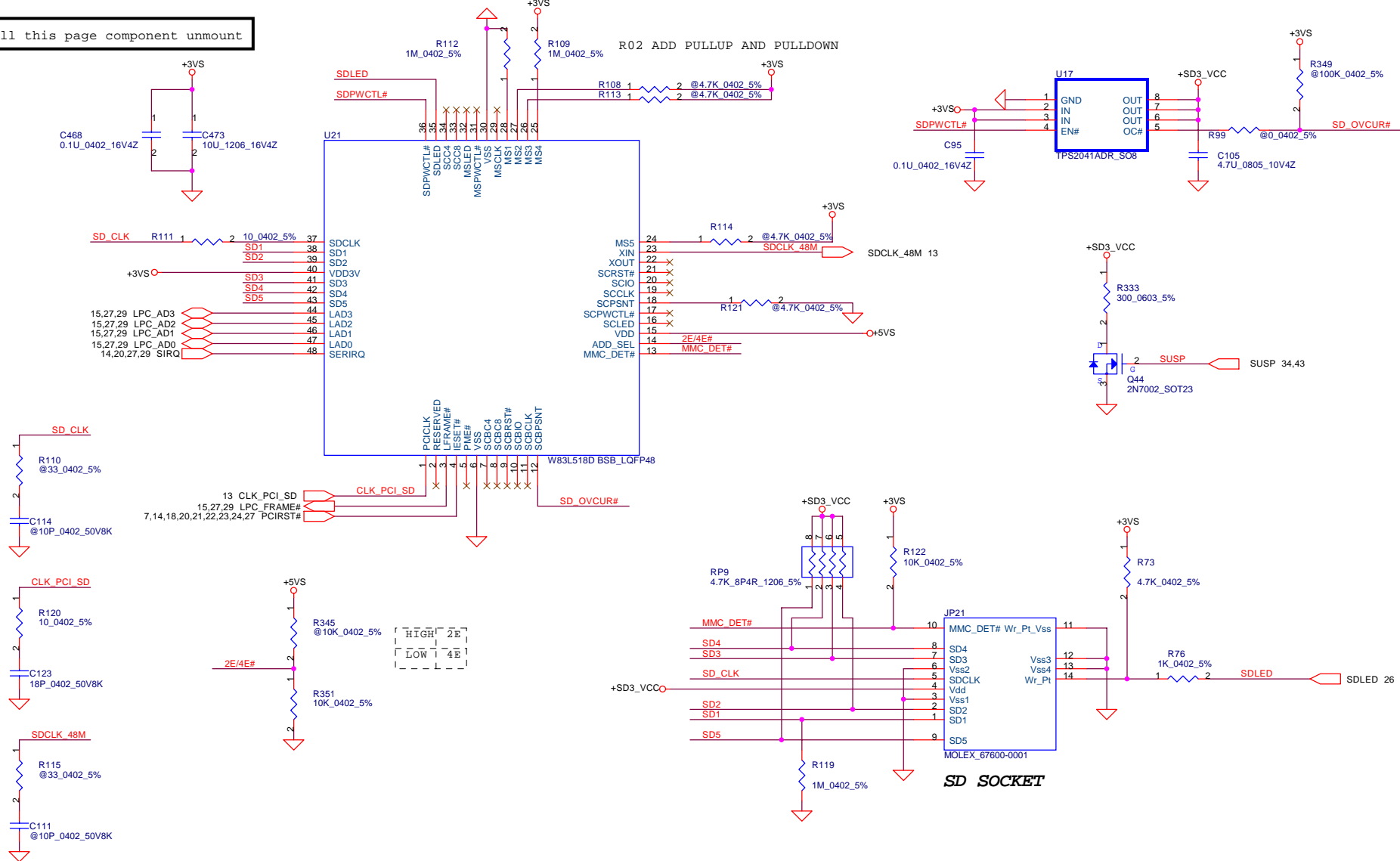


Compal Electronics, Inc.

Title			Mini PCI Slot
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FOR ABO: all this page component unmount



Compal Electronics, Inc.

Title	SD CARD Controller/Socket
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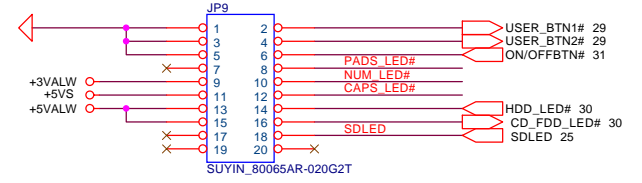
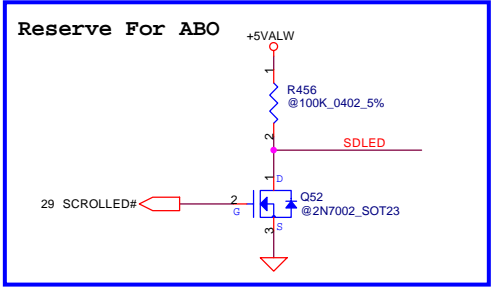
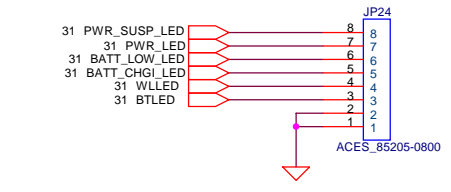
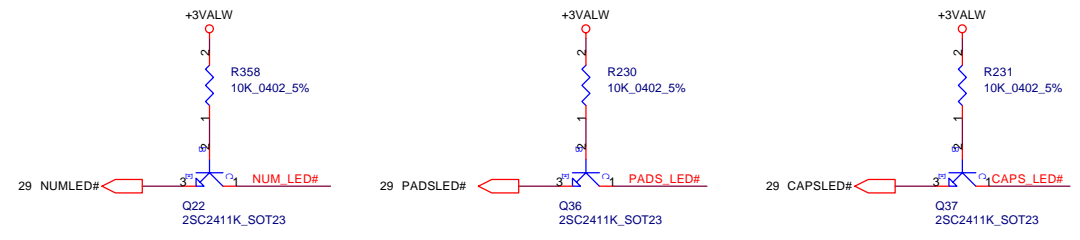
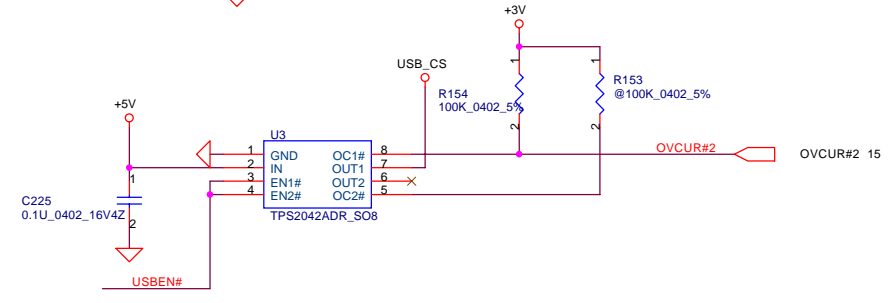
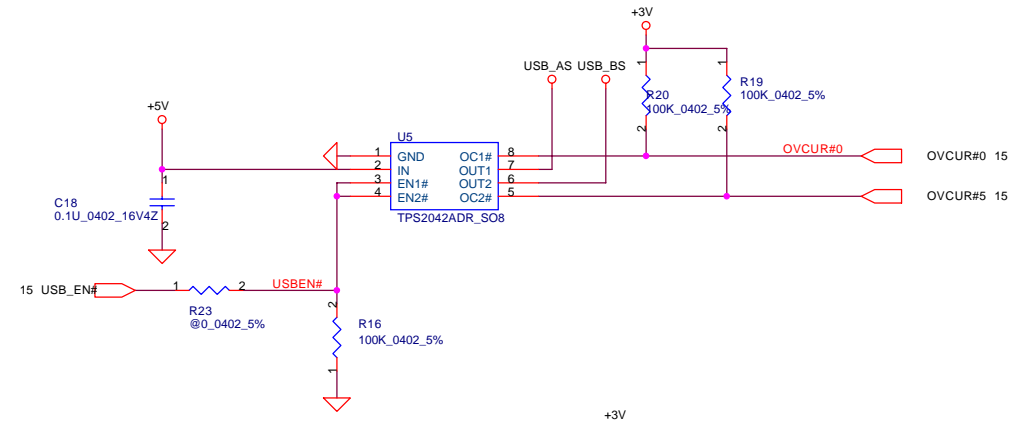
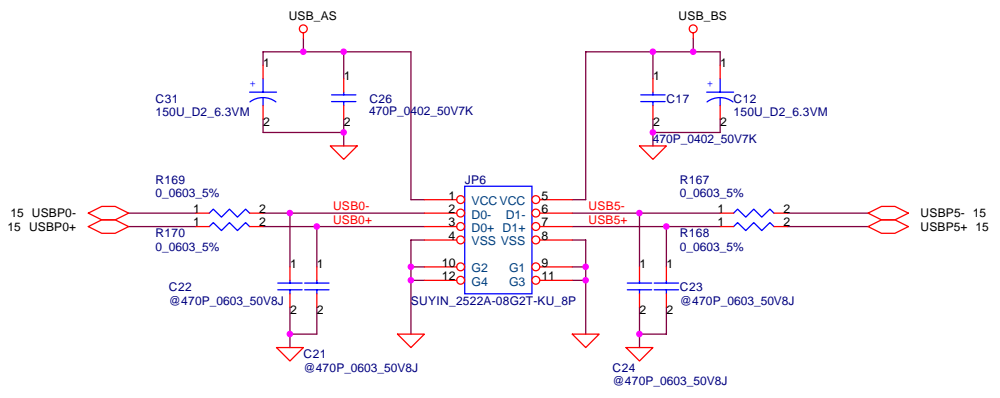
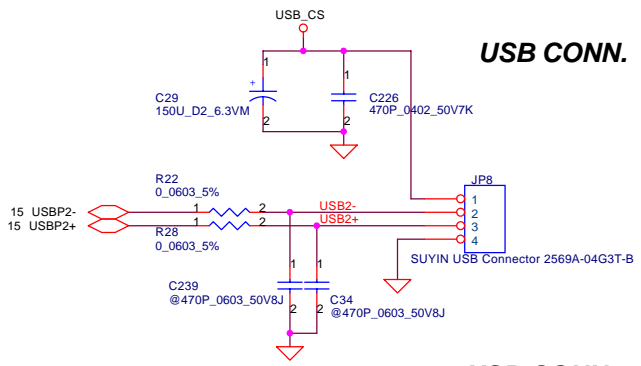
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Date: Friday, January 09, 2015

Rev
1.0

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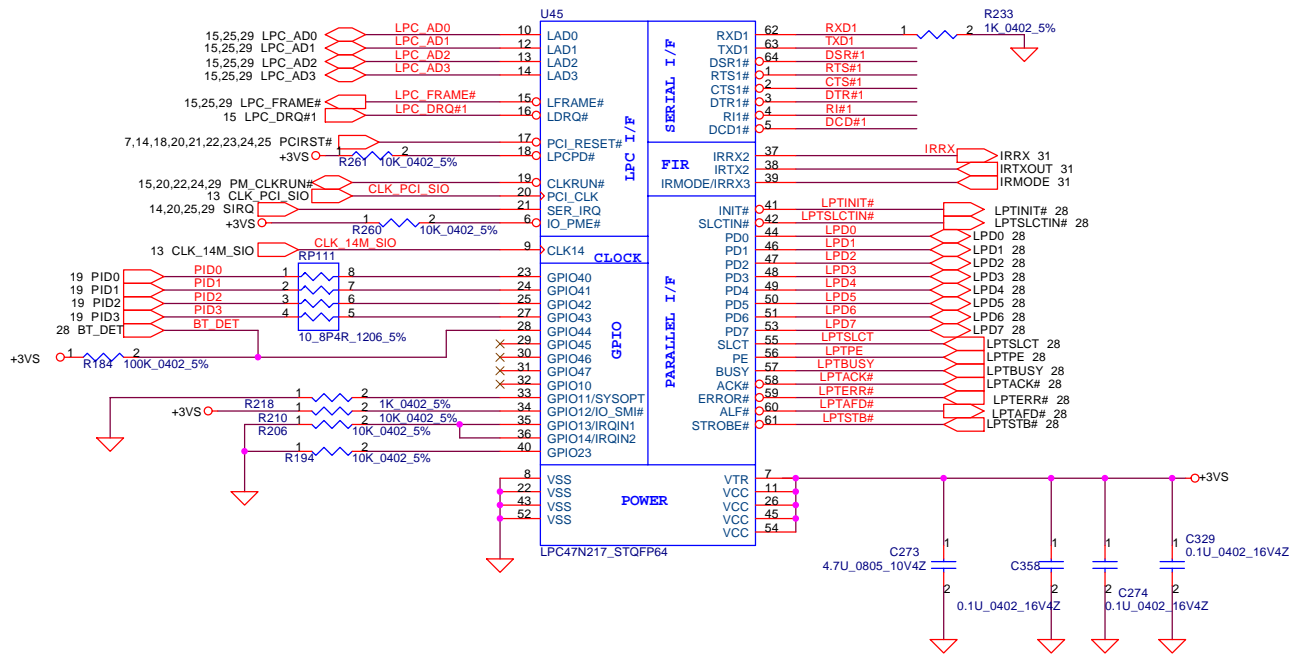
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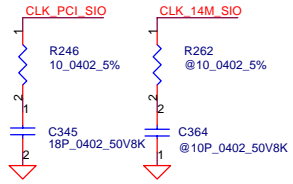
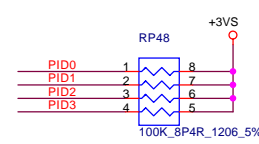
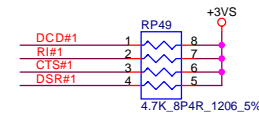
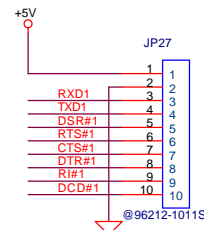
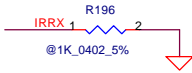
Compal Electronics, Inc.			
Title			
USB & LED			
Size	Document Number		Rev
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SUPER I/O SMsC FDC47N227



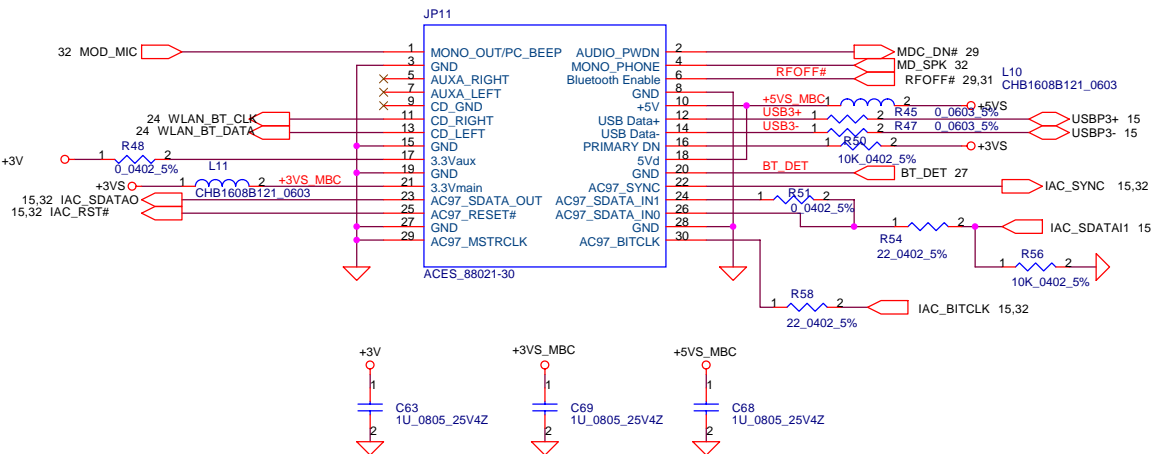
Base I/O Address
* 0 = 02Eh
1 = 04Eh



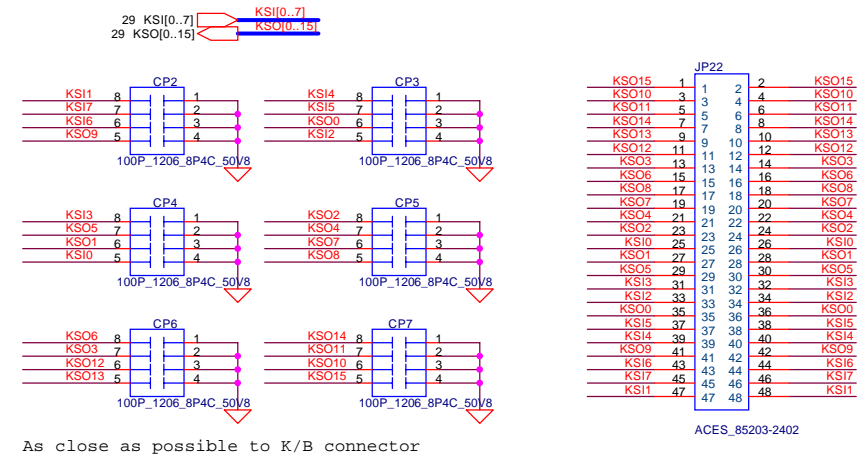
Compal Electronics, Inc.			
SUPER I/O			
Size	Document Number	Rev	
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MBC CONN.

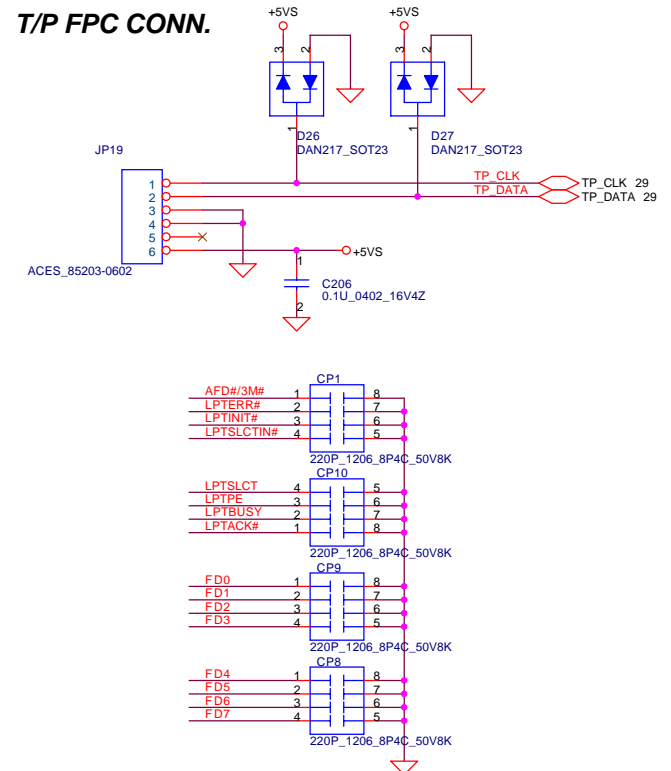


INT_KBD CONN.

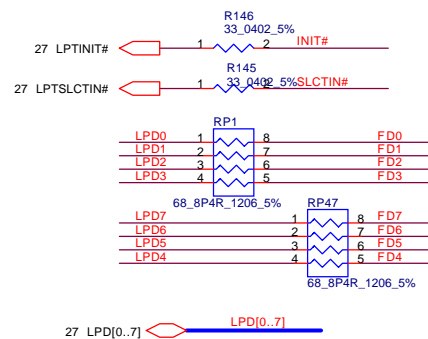
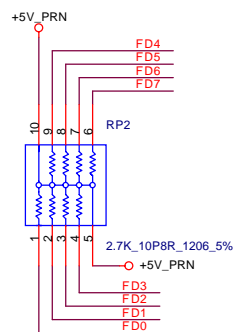
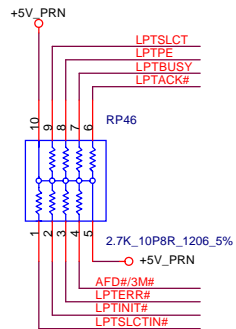
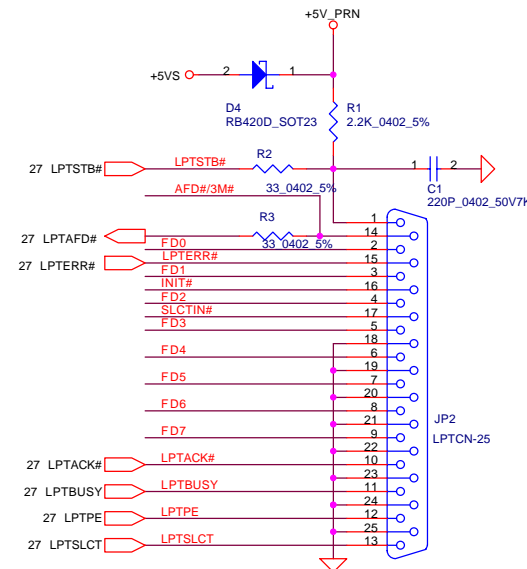


As close as possible to K/B connector

T/P FPC CONN.



PARALLEL PORT

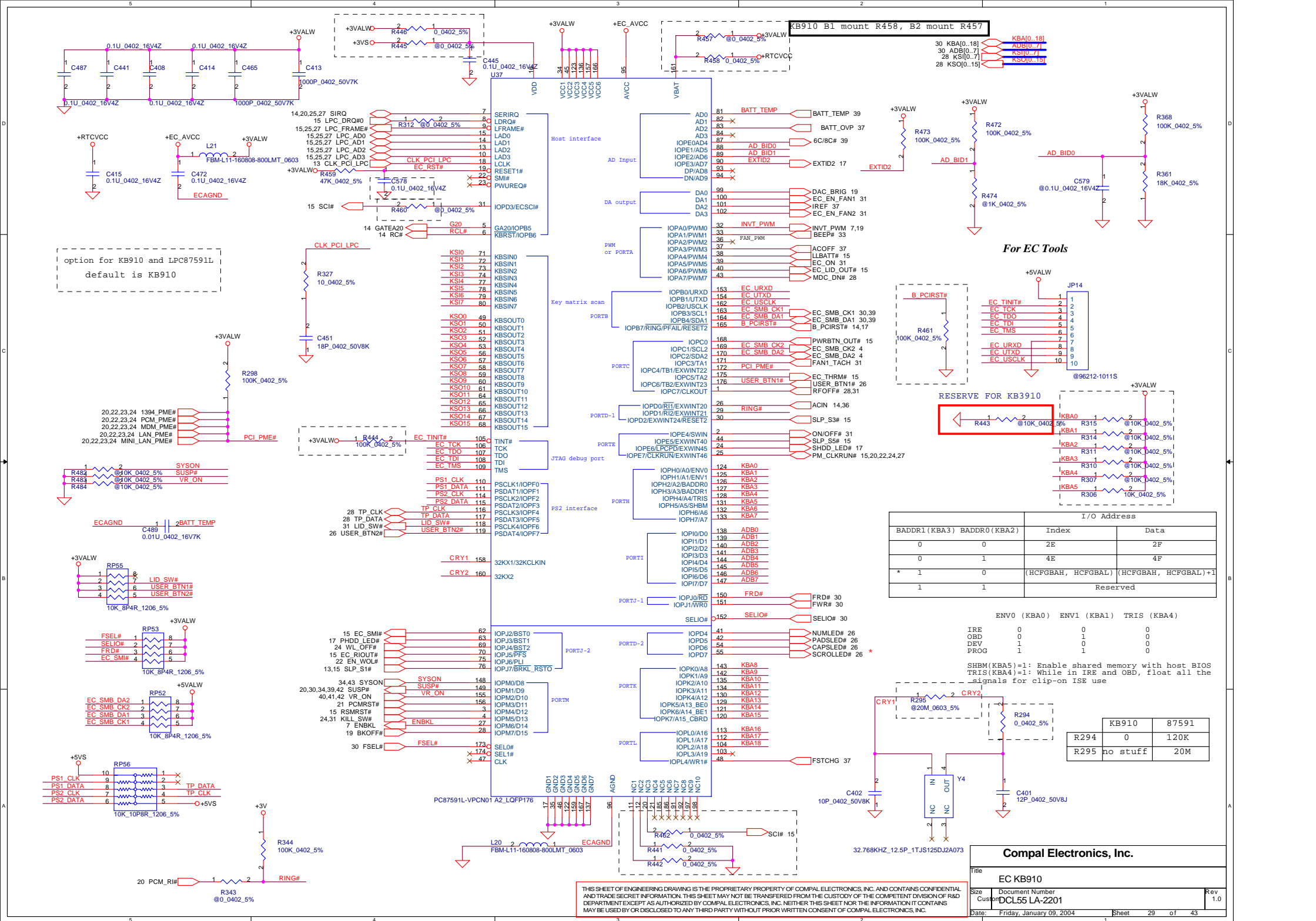


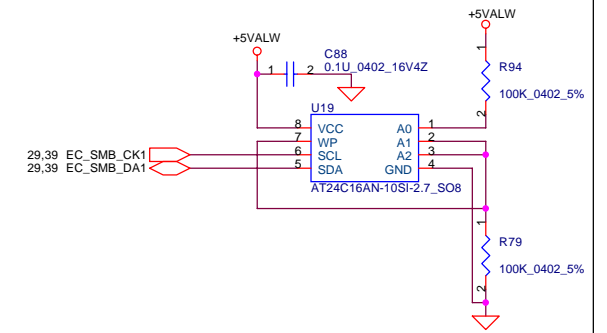
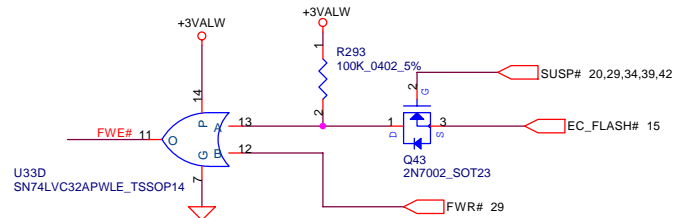
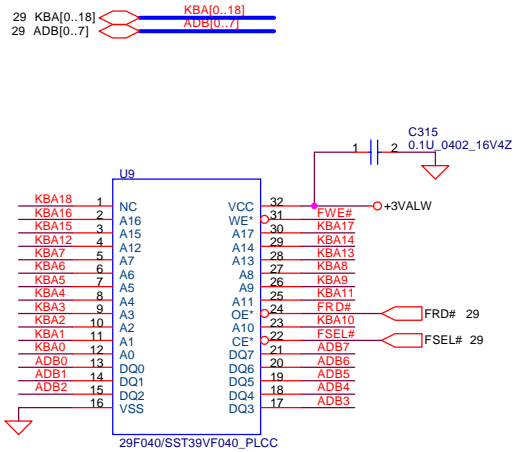
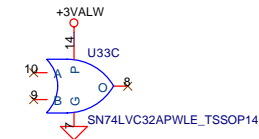
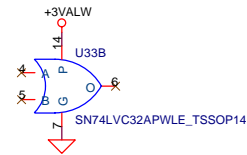
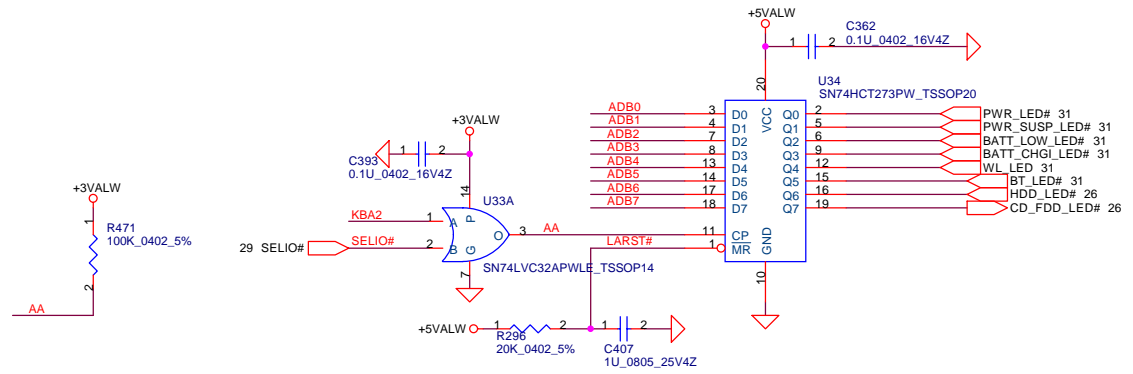
27 LPD[0..7] → LPD[0..7]

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Title	PARALLEL/MDC PORT		
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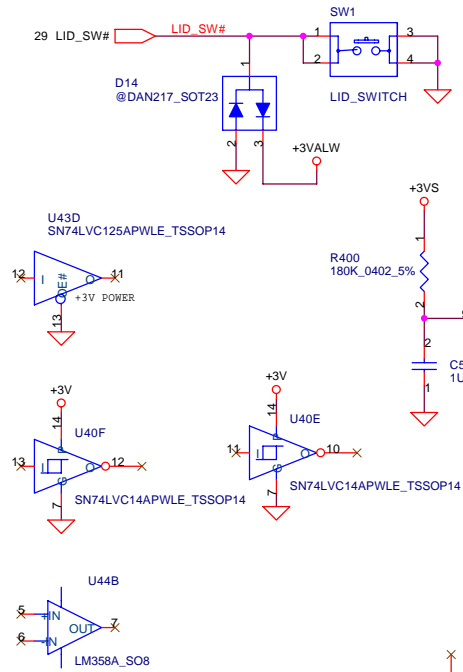


Compal Electronics, Inc.

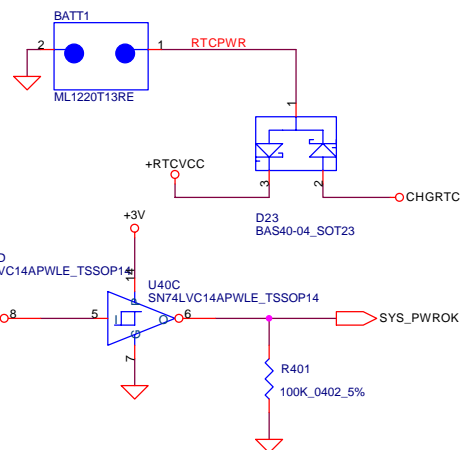
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BIOS & EXT. I/O PORT			
Size	Document Number	Rev	
B	DCL55 LA-2201	1.0	
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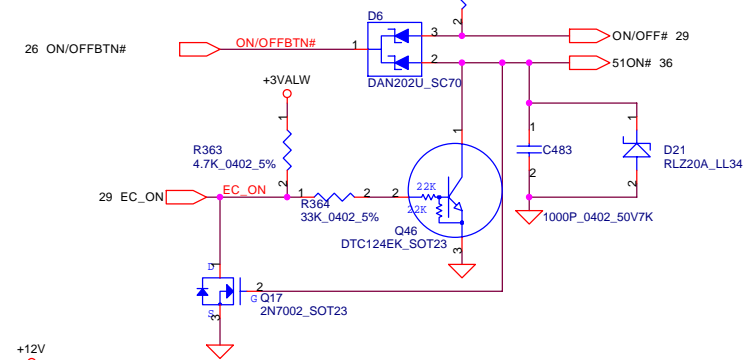
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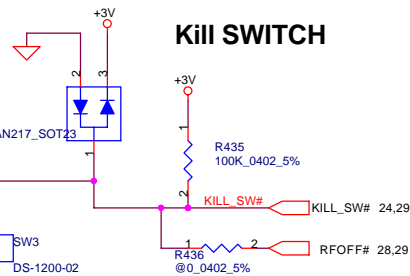
RTC Battery



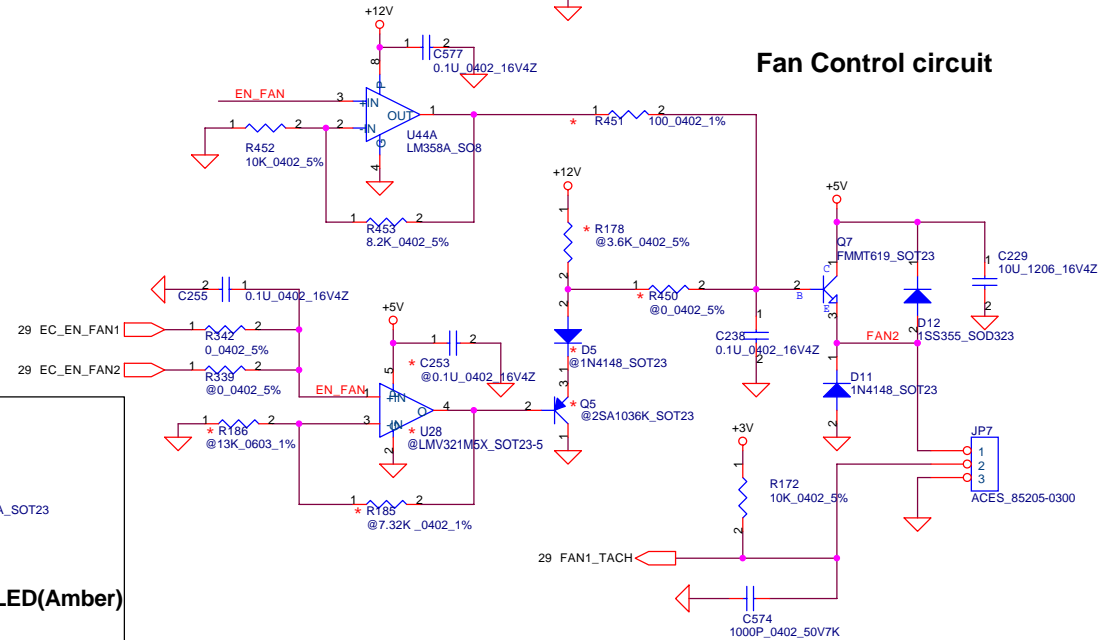
Power BTN



Kill SWITCH

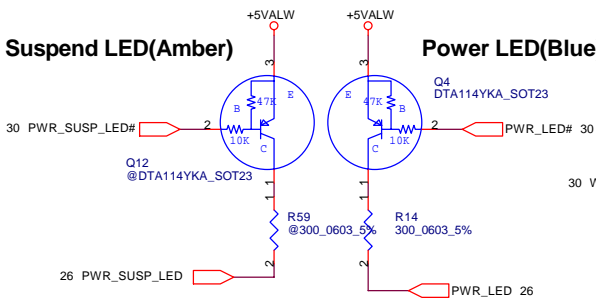


Fan Control circuit



Suspend LED(Amber)

Power LED(Blue)

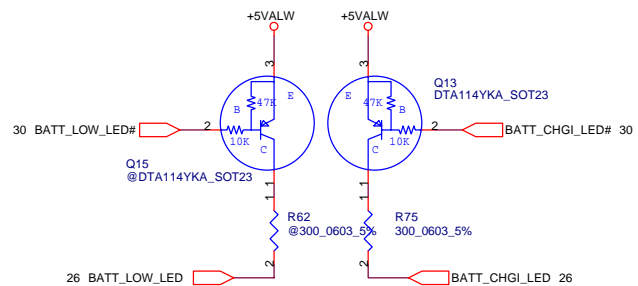


Wireless LED(Amber)

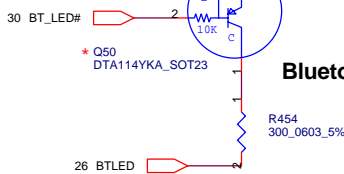


BATT Low LED(Amber)

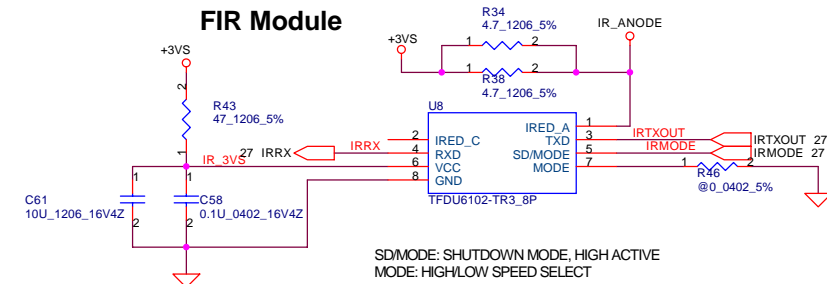
BATT Charge LED(Blue)



Bluetooth LED(Blue)



FIR Module

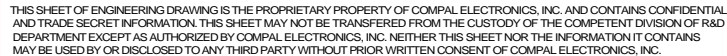


Compal Electronics, Inc.

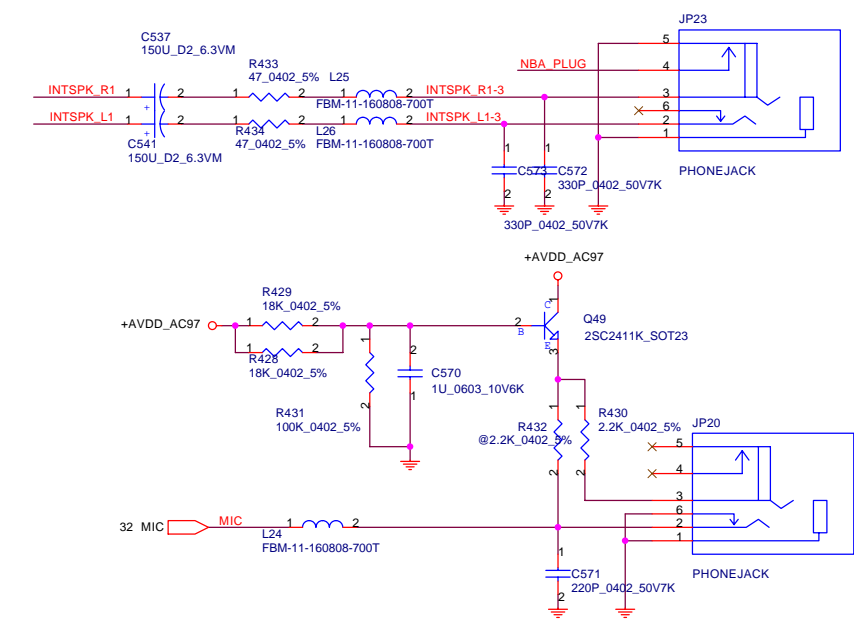
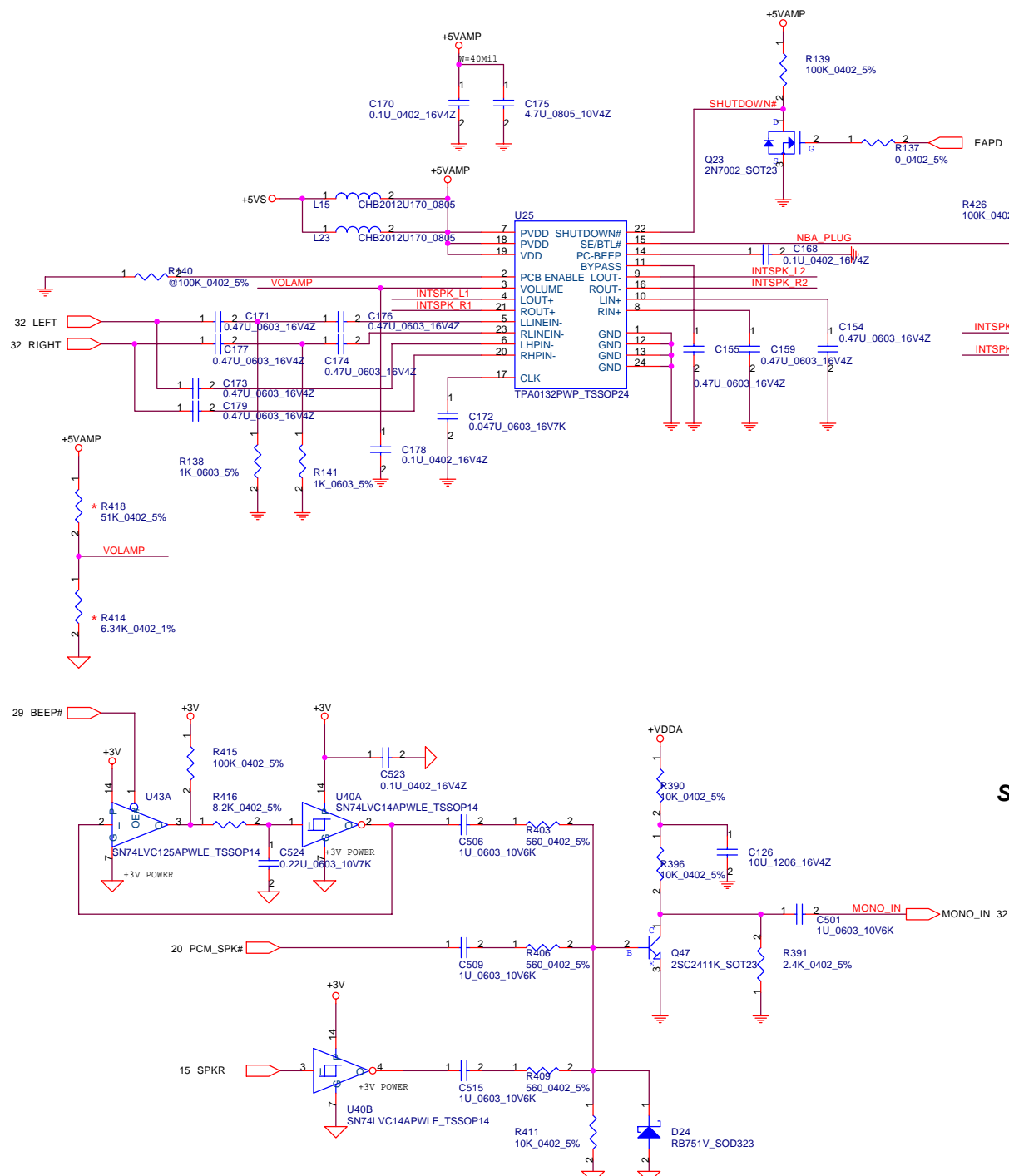
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Size	Document Number	Rev	
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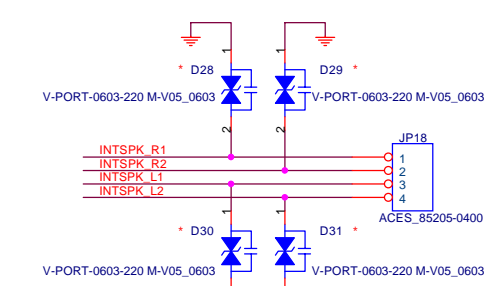
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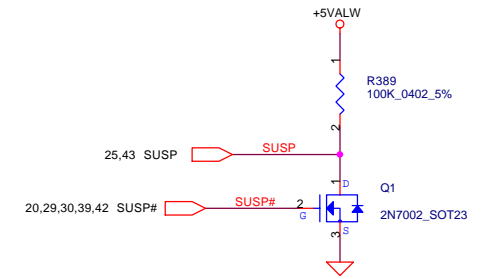
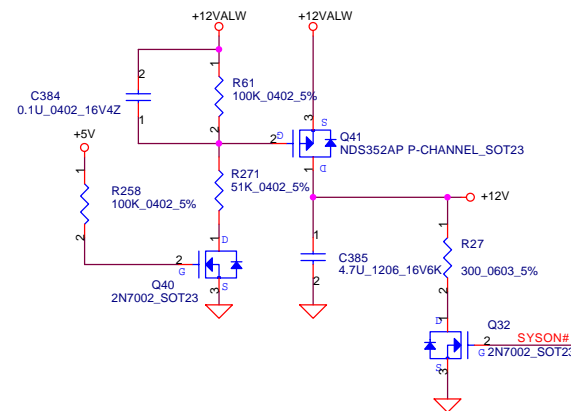
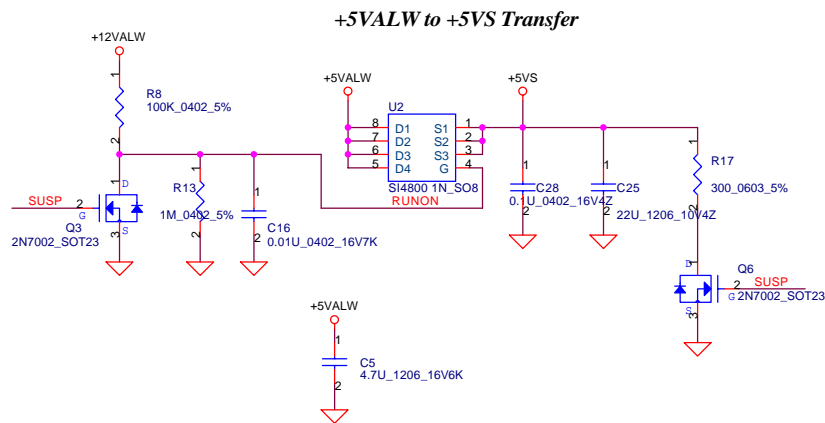
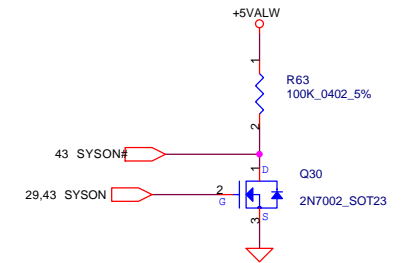
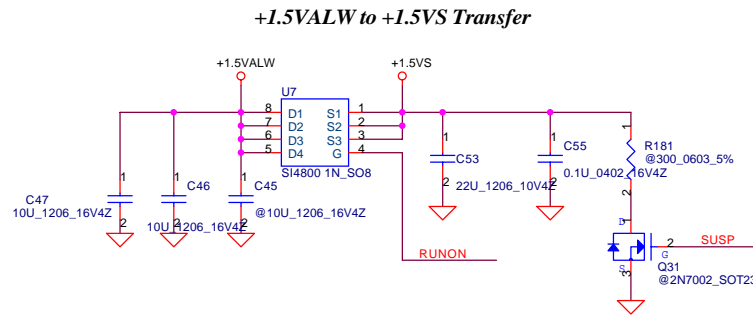
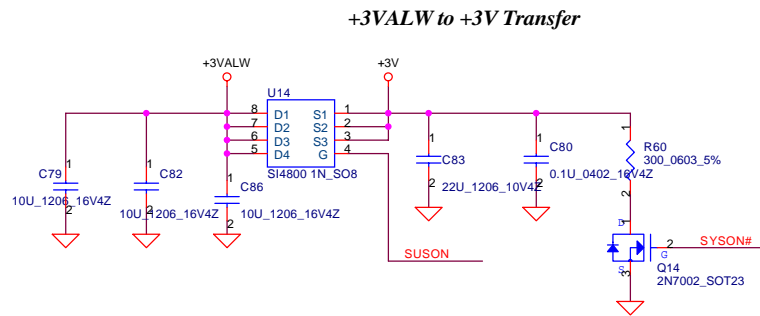
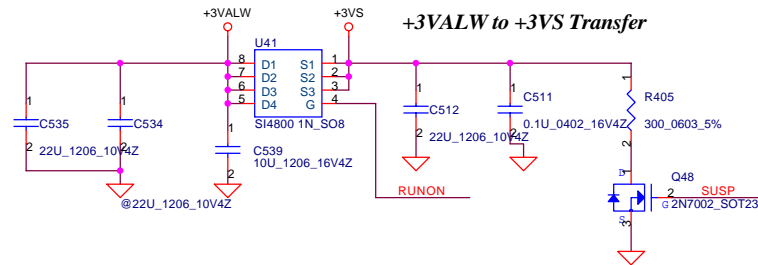
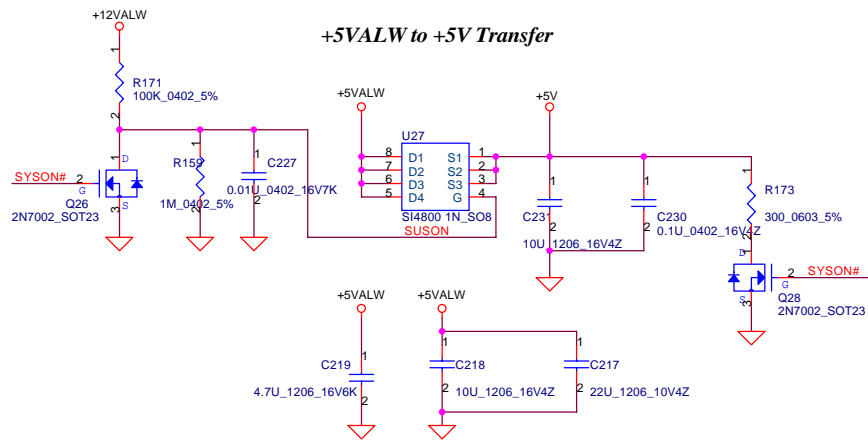


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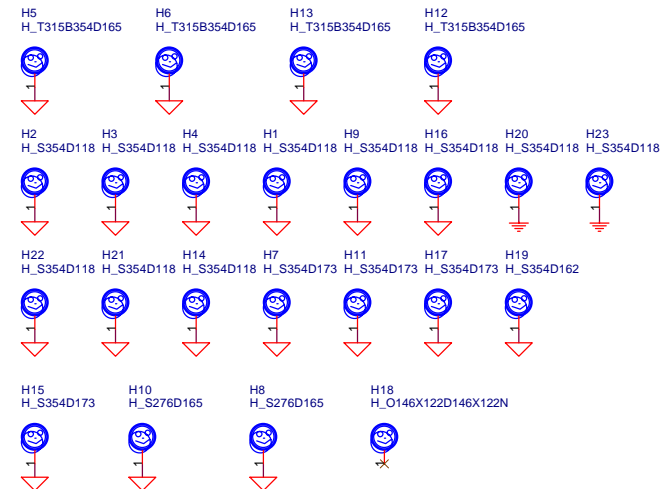
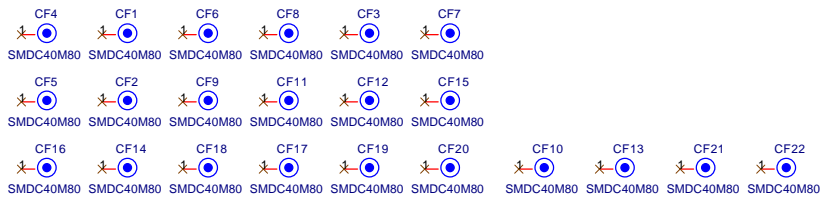
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Compal Electronics, Inc.			
Title			
AMP & Audio Jack			
Size	Document Number	Rev	
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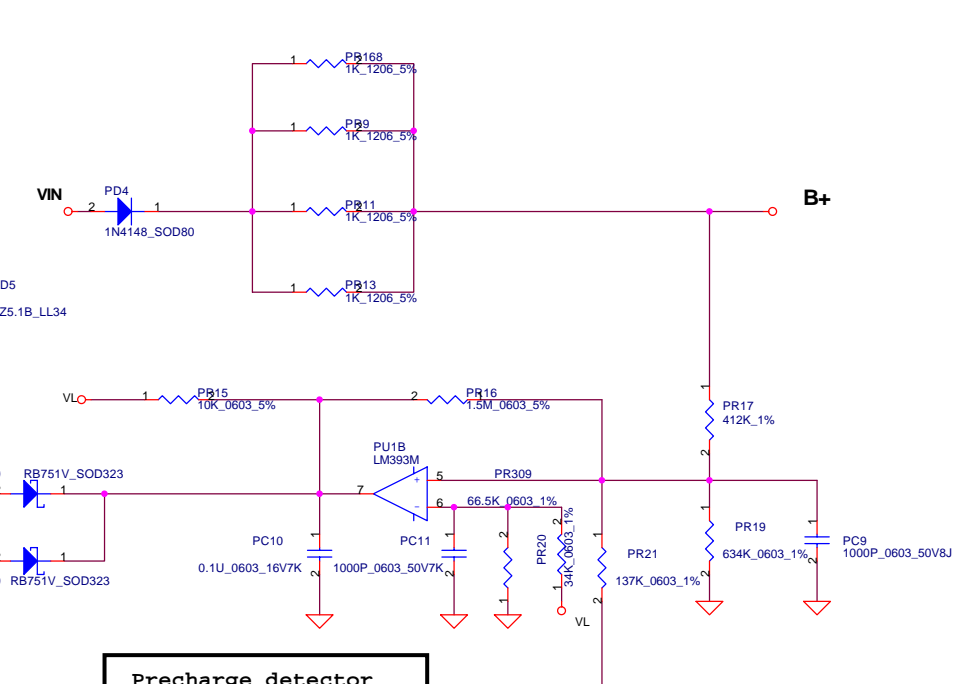
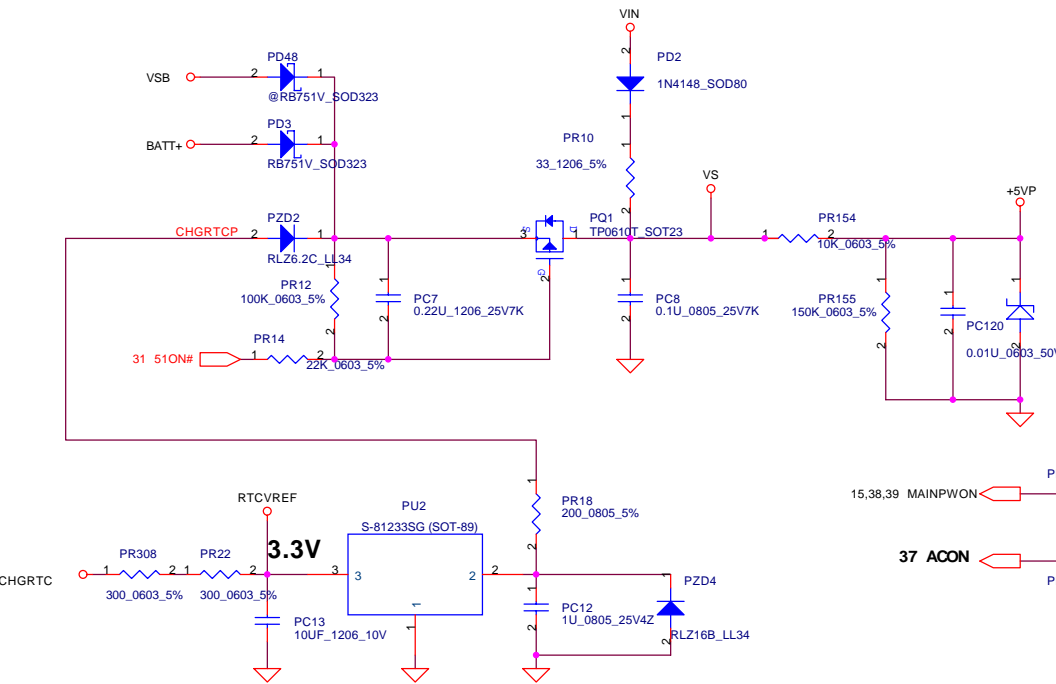
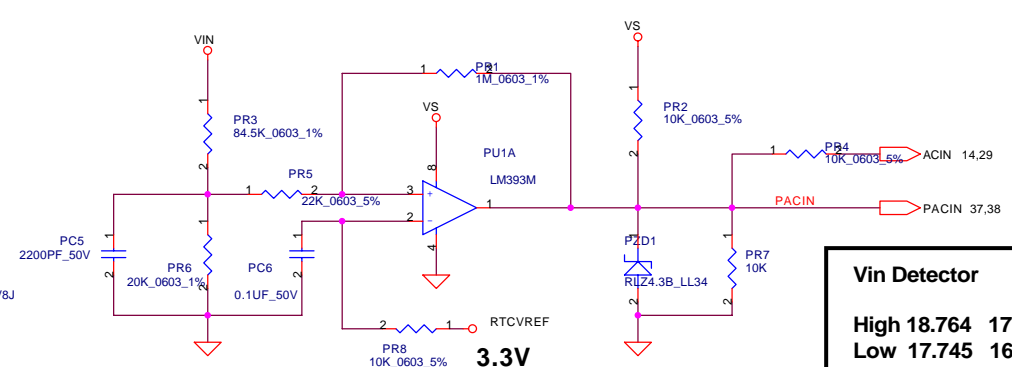
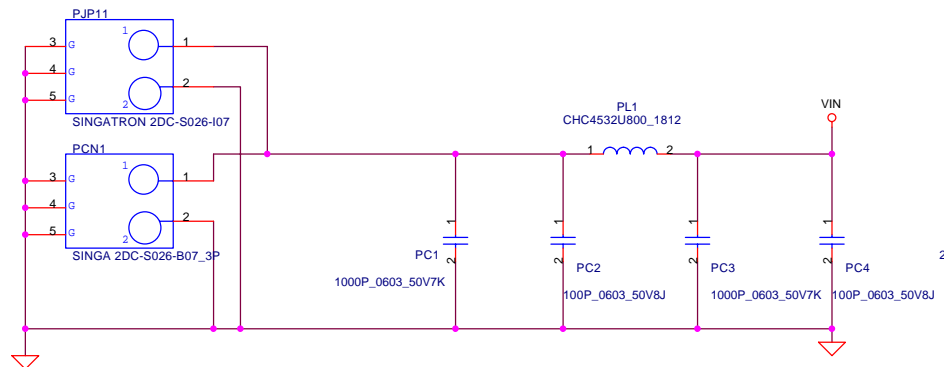
Compal Electronics, Inc.			
Title			
DC/DC Circuit Interface			
Size	Document Number	Rev	
	DCL55 LA-2201	1.0	
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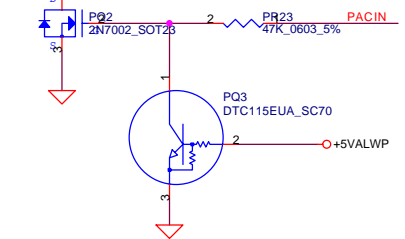
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Compal Electronics, Inc.			
Title		Skew Hole	
Size	Document Number		Rev
	DCL51 LA-1881		1.0
Date:	Friday, January 09, 2004	Sheet	35 of 45



Precharge detector AC ADAPTOR		
16.69	16.05	15.42
15.6	15.02	14.35

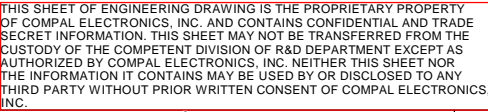
Precharge detector AC ADAPTOR		
6.33	6.12	5.92
5.227	5.09	4.85

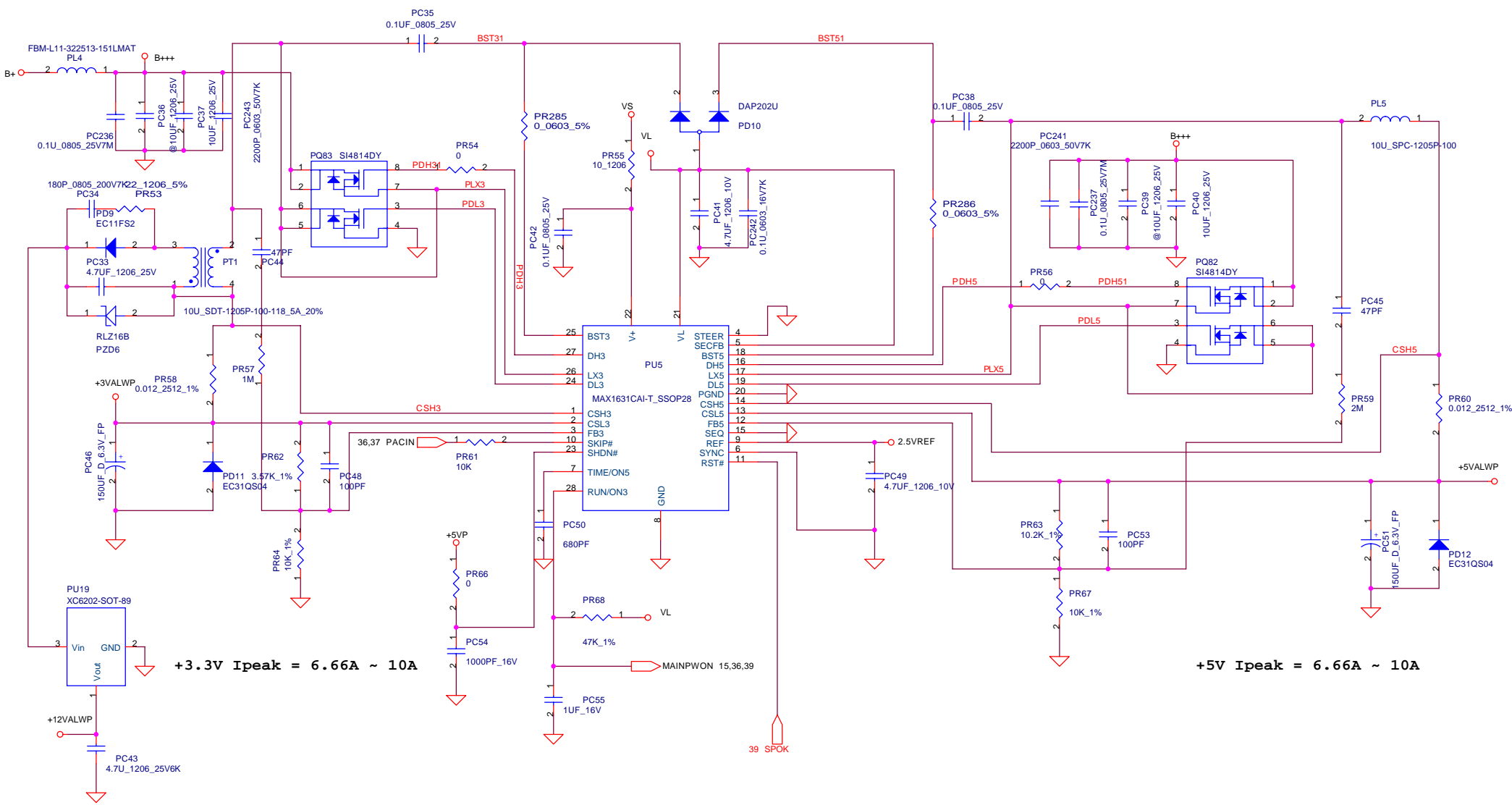


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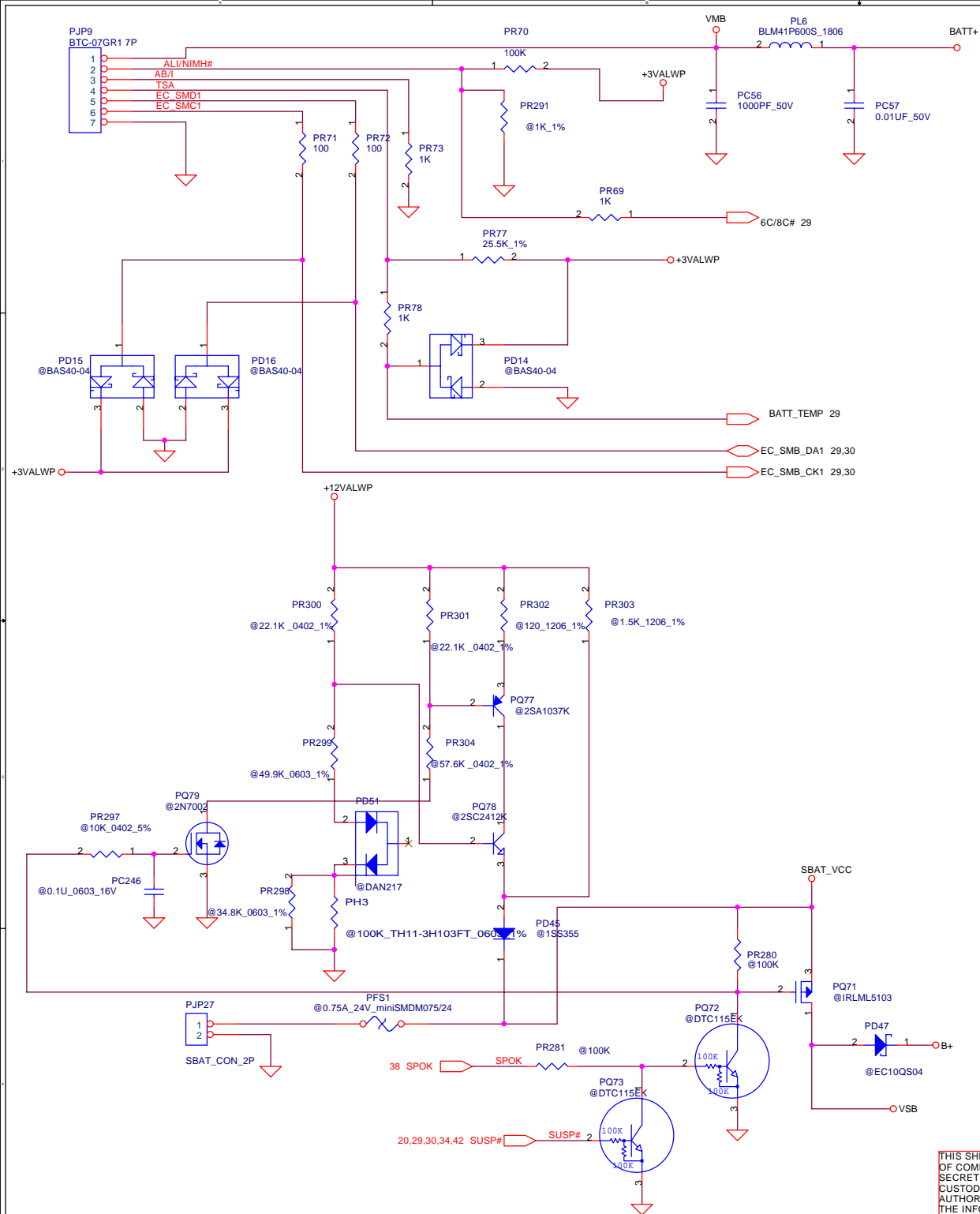
Compal Electronics, Inc.		
Title DCIN & DETECTOR		
Size B	Document Number DCL55 LA-2201	Rev 1.0
Date: Friday, January 09, 2004	Sheet 36	of 45

Rev
1.0

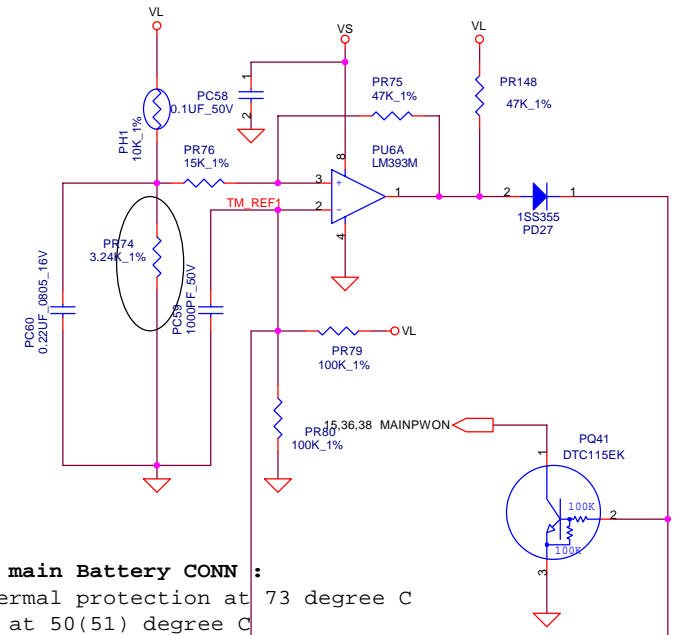


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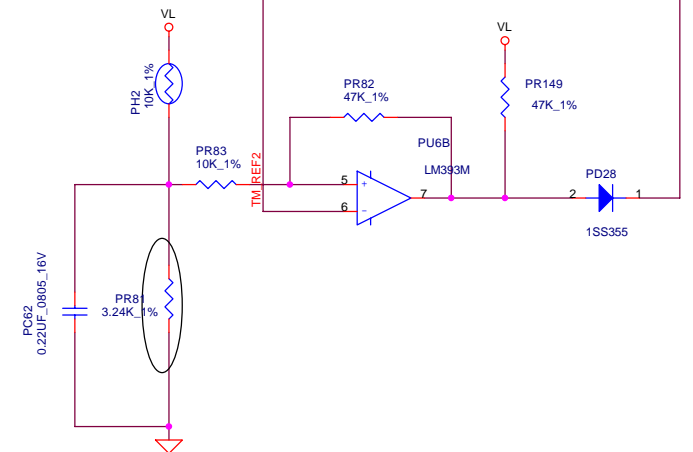
Compal Electronics, Inc.			
Title	5V/3.3V/12V		
Size	Document Number		
B	DCL55 LA-2201		
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Rev	1.0		



PH1 under CPU botten side :
CPU thermal protection at 82 degree C
Recovery at 48 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 73 degree C
Recovery at 50(51) degree C

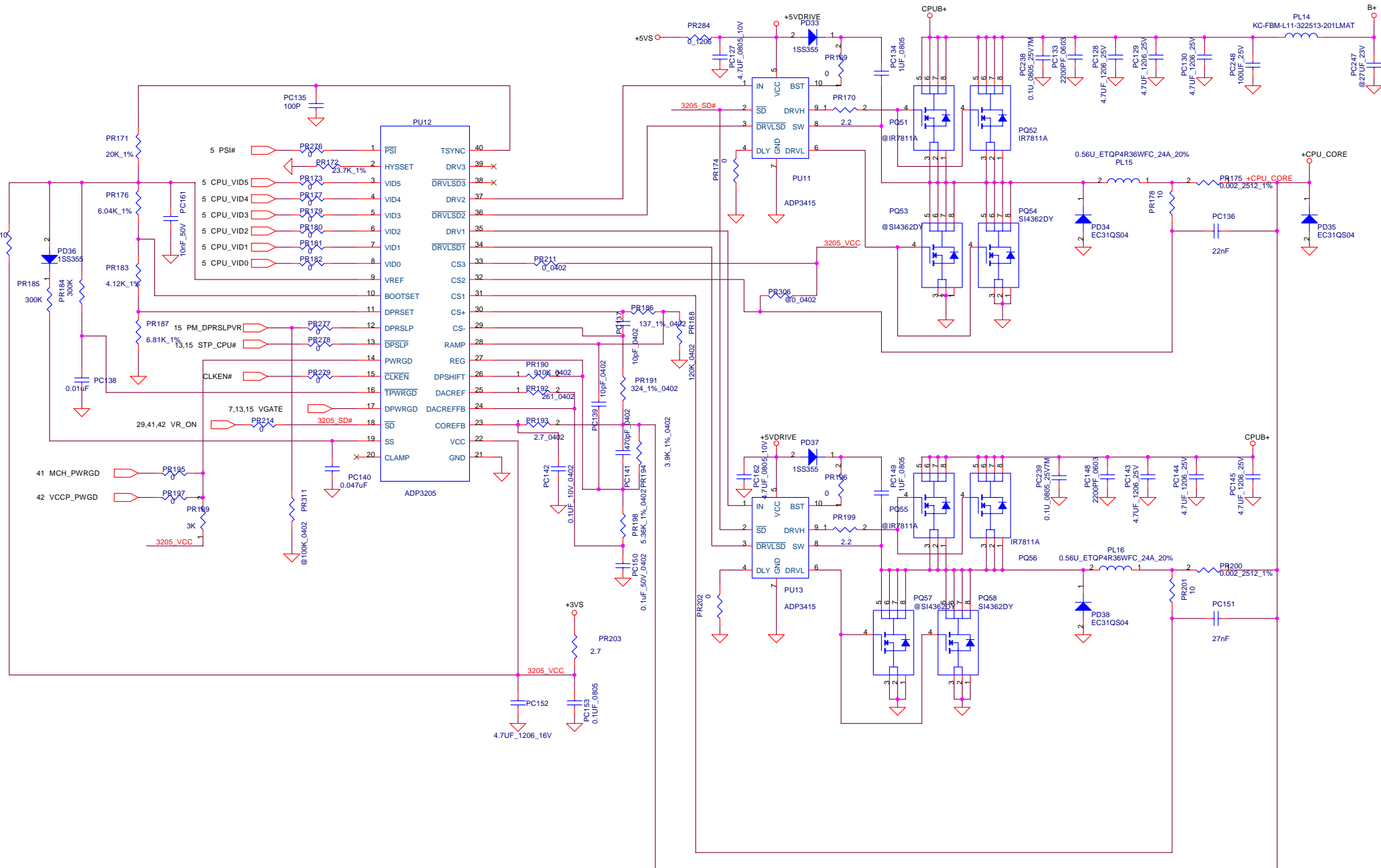


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Title			BATTERY CONN / OTP/1.2V
Size	Document Number	Rev	
B	DCL55 LA-2201	1.0	
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CPU-CORE



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Compal Electronics, Inc.

+VCC_H_CORE

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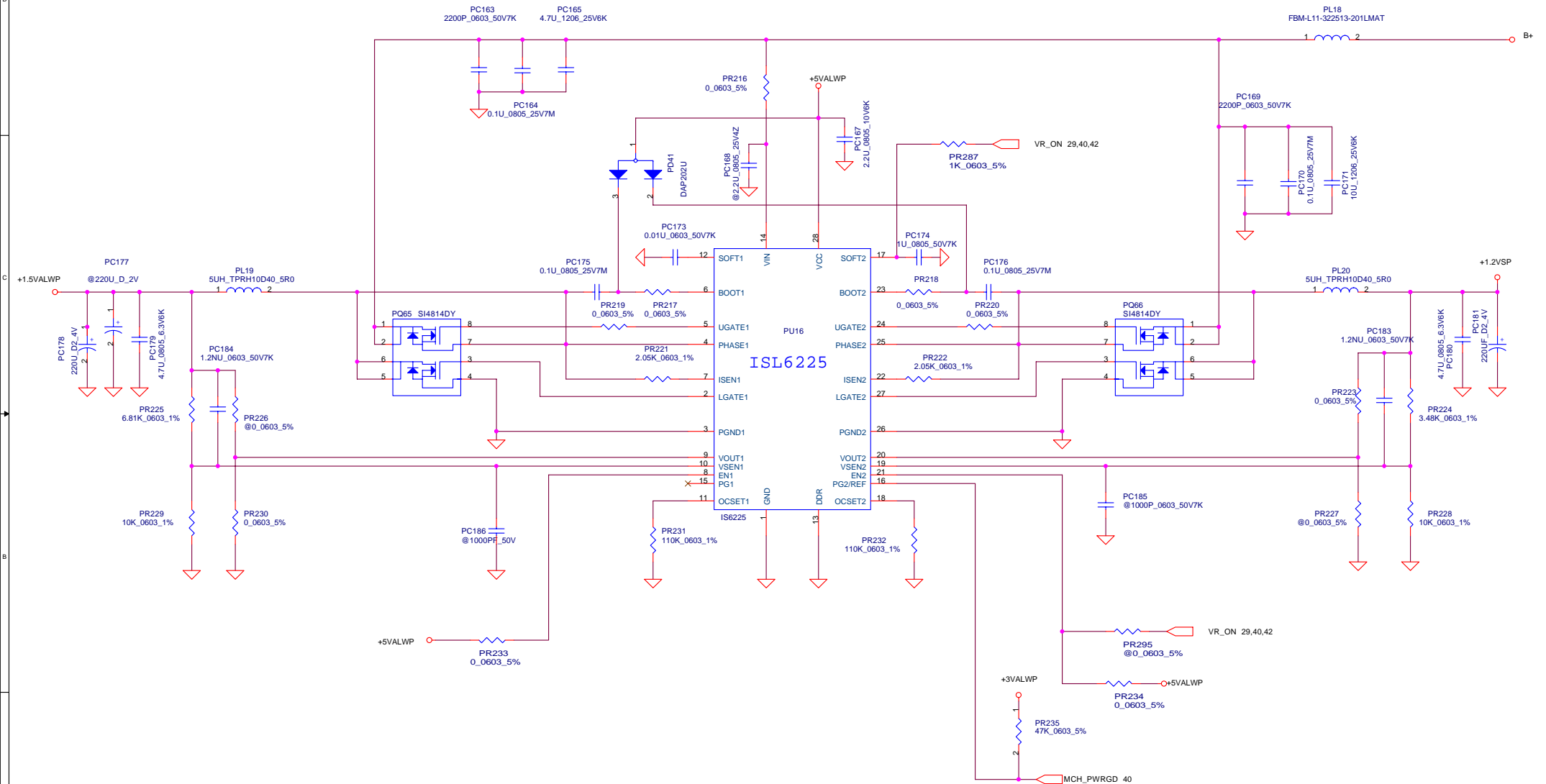
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1.0

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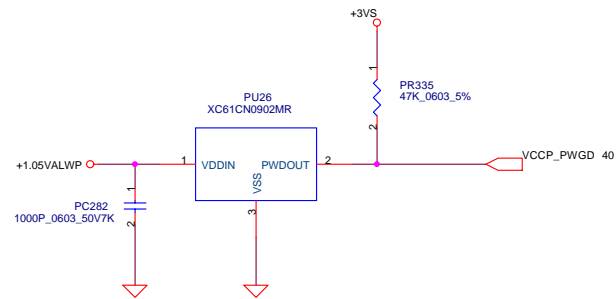
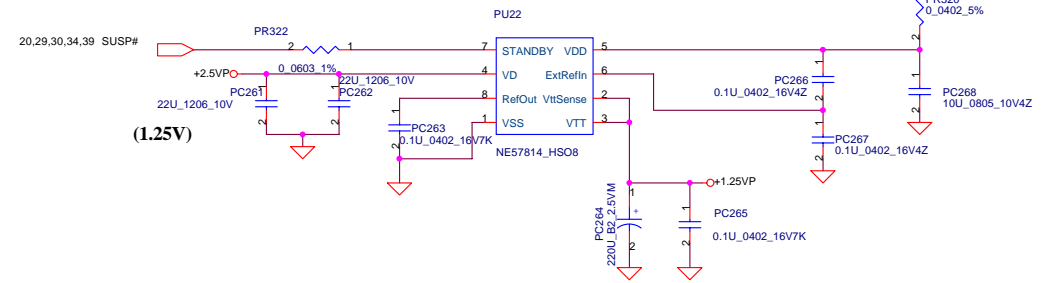
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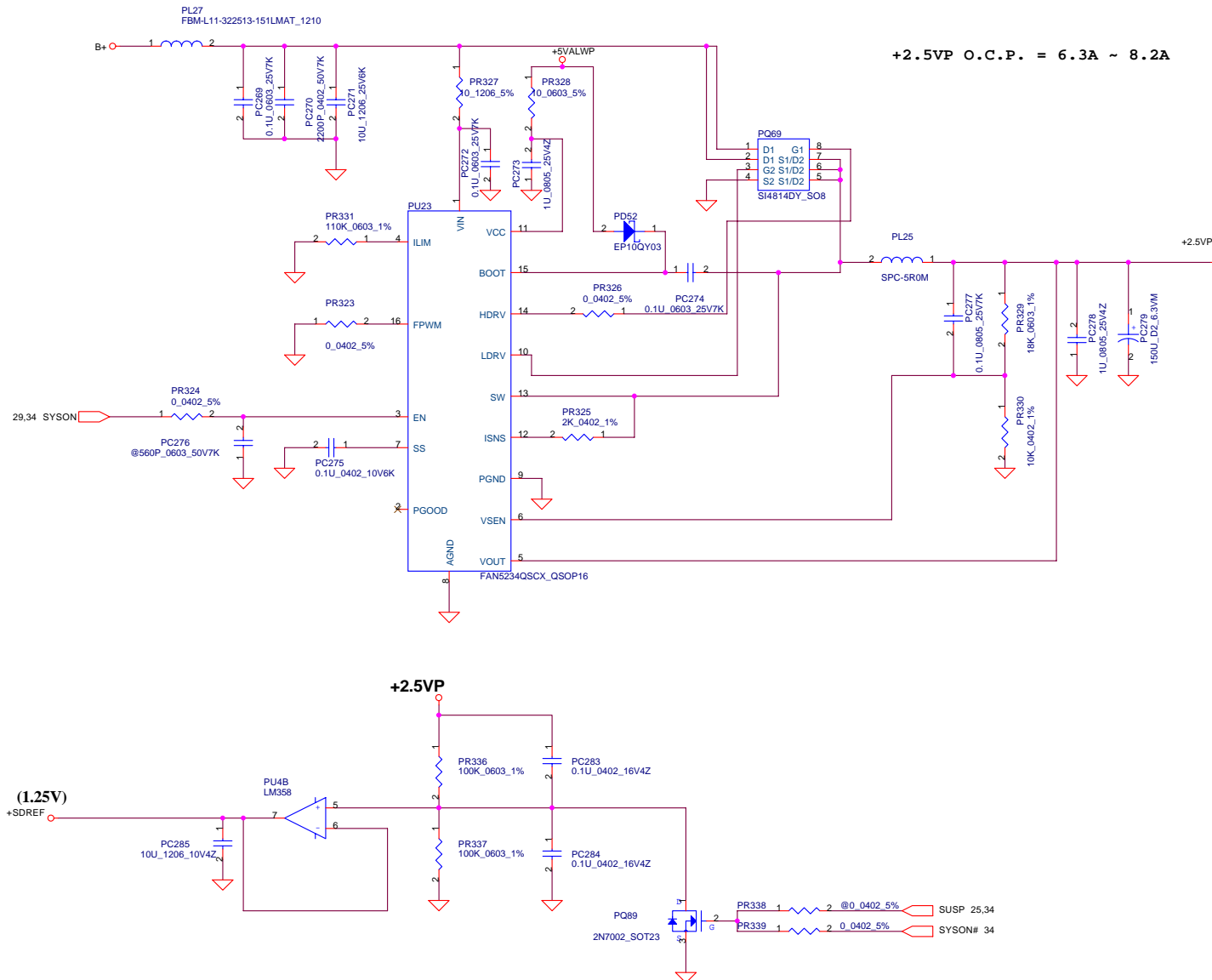


Compal Electronics, Inc.

Title			
1.5V & 1.2V			
Size	Document Number		Rev
B	DCL55 LA-2201		1.0
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Compal Electronics, Inc.			
Title			
2.5V & 1.25V			
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		Set c4 mode controlled by bios based difference CPU		40	DELETE PR311:100K ; ADD PR277:0		PVT
2		Modify 1.05VP voltage level		42	1. change PR314 to 200k		PVT
3		modify 1.05VP,1.8VP soft start time		42	add PC253, PC258 Tto be 0.1U		PVT
4		add +SDREF signal circuit		43	add PR339:0; PQ89: 2N7002; PC283,PC284 :0.1U 16V;PR336,PR337:100K;PC285:10U 1206		PVT
5		Add one set power good:VCCP_PWGD		42,41	ADD LDO PU26 :XC61CN;PR335:47K;PC282:1000P 50V,PCHANGE R235 FROM 10K TO 47K		PVT
6							
7							
8							
9							

Compal Electronics, Inc.

Title

PIR (PWR)

Size

Document Number

DCL55

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1.0

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		reserve +SDREF signal circuit		8	reserve R477,R479		PVT
2		reserve +SDREF signal circuit		10	reserve R480,R481		PVT
3		EMI performance		8	change C420_net from MRCOMP to +2.5V		PVT
4		reserve syson,susp#,vr_on pull low resister		29	reserve R482,R483,R484		PVT
5		cost down			change L18,L19,L14,L13,L12,L8,L9,L7 to 0 ohm del C534,C45		PVT
6		board version update		29	change R361 from 8.2k to 18k		
7		for customer request			del TV_out , 1394 funtion		
8							
9							